Monolithic Silicon Pixel Detectors in HEP – Overview and Status

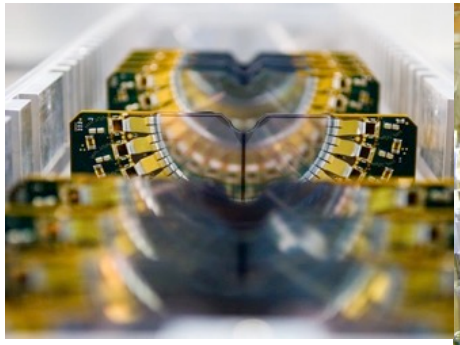
Outlook

- Monolithic Pixel Detectors
- The ALICE ITS
- Further Developments of Monolithic Pixel Detectors
- Summary

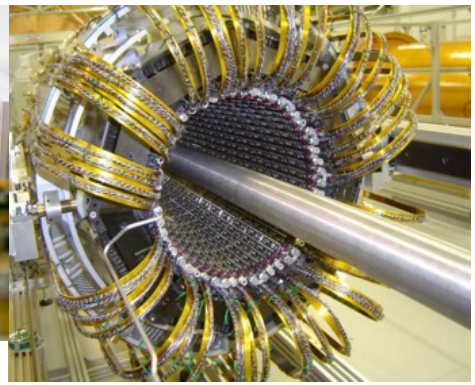
Silicon Tracking Detectors

- Complex systems operated in a challenging high track density environment
- Innermost regions usually equipped with pixel detectors

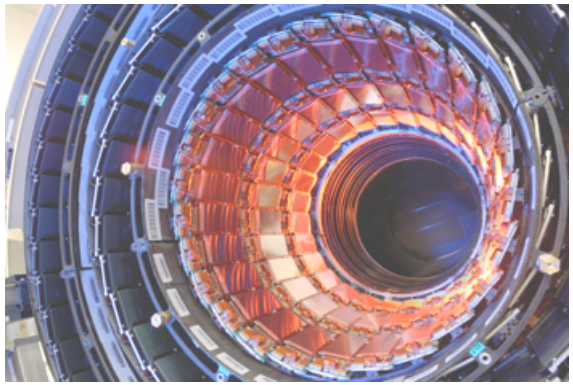
ALICE **Pixel** Detector



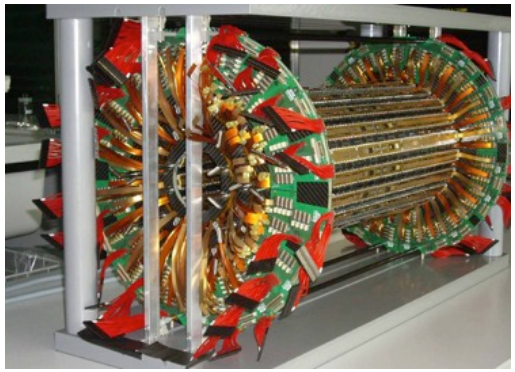
LHCb VELO



ATLAS **Pixel** Detector



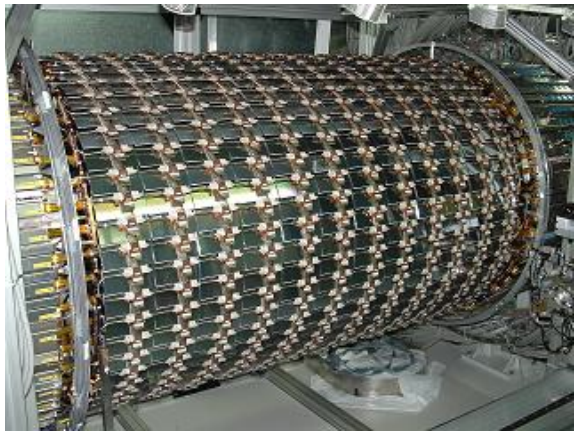
CMS Strip Tracker IB



CMS **Pixel** Detector

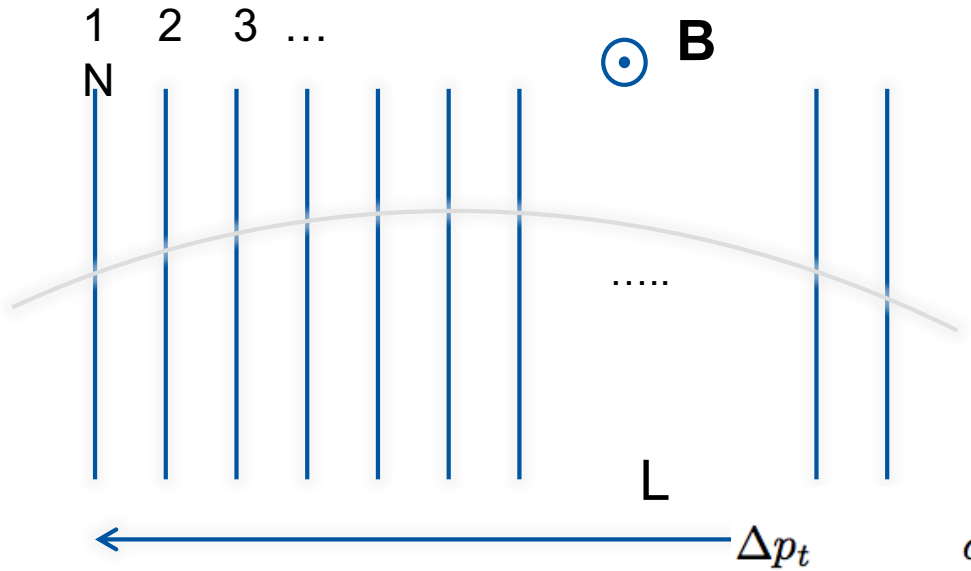
ALICE Drift Detector

ALICE Strip Detector



ATLAS SCT Barrel

Tracking – Momentum Resolution



σ … point resolution/plane

X_{tot}/X_0 … total material budget

Position Resolution

Pixel = high spatial resolution

O(10μm) on hybrid and down to O(1-3μm) on MAPS

Multiple Scattering

Pixel = light detectors

Thin detectors on light carbon fibre supports O(1-2% X/X_0 per layer)

$$\frac{\Delta p_t}{p_t} = \frac{\sigma[m]\, p[\mathrm{GeV/c}]}{0.3\, B[T]\, L^2[m^2]} \sqrt{\frac{720\,(N-1)^3}{(N-2)\,N\,(N+1)\,(N+2)}}$$

$$\approx \frac{\sigma[m]\, p[\mathrm{GeV/c}]}{0.3\, B[T]\, L^2[m^2]} \sqrt{\frac{720}{N+4}}$$

$$\frac{\Delta p_t}{p_t} = \frac{0.0136}{0.3\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7}\,\frac{12+(N-1)N^2(N+1)}{(N-2)N(N+1)(N+2)}}$$

$$\approx \frac{0.0136}{0.3\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7}}$$

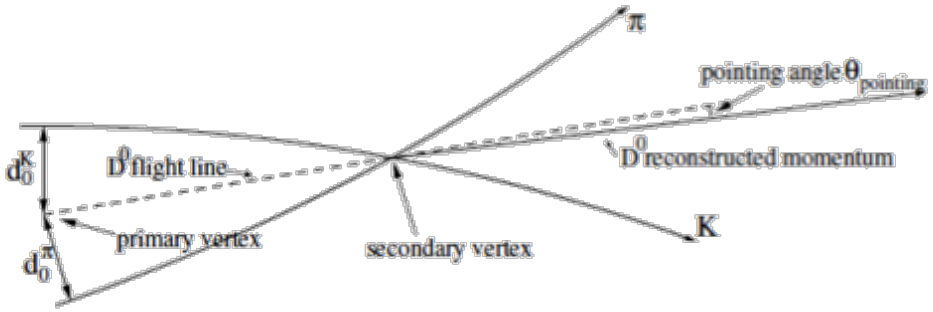
$$\approx \frac{0.0542}{\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}}$$

R.L. Gluckstern, NIMA 24 (1963), 381-389

Impact Parameter

- Excellent impact parameter resolution is mandatory for reconstruction of heavy flavor vertex (c and b vertex)

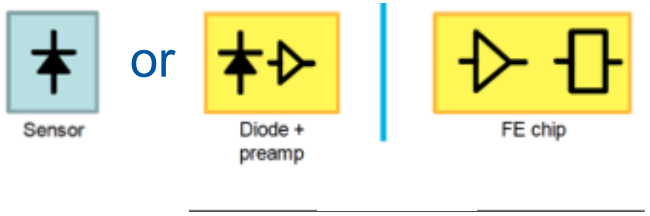
- Secondary vertices reconstruction strongly depends on impact parameter resolution

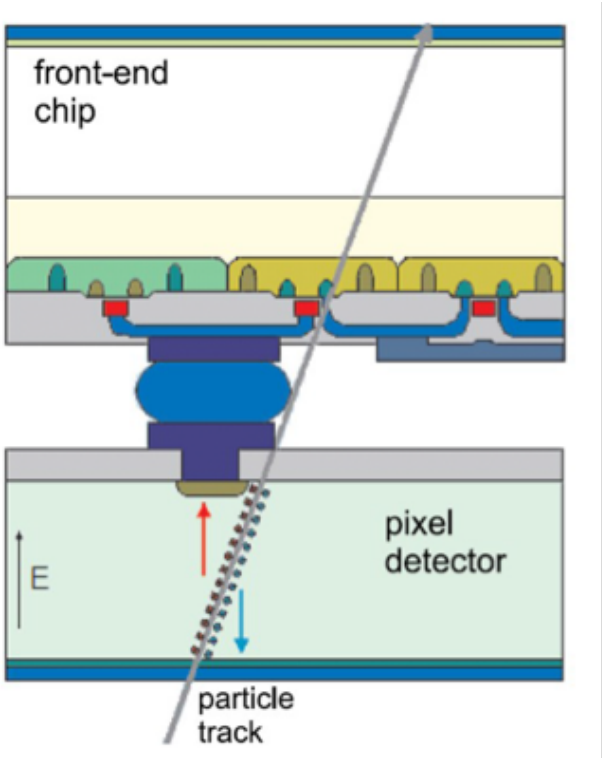


- Impact parameter resolution is strongly effected by
  - **Intrinsic point** resolution and alignment at higher momentum
  - **Multiple scattering in detector material** (in particular for low pt tracks)

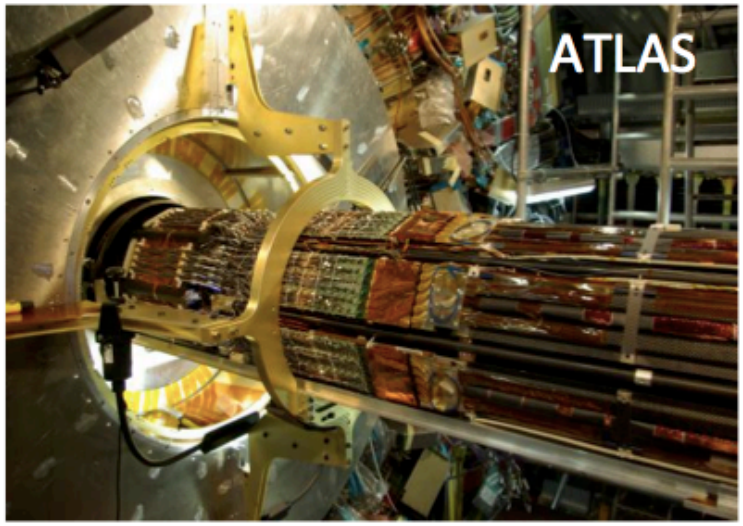
Hybrid Pixels

- Sensor and ASIC are independent units
- Complex readout with zero-supression and in-pixel hit buffering
- Separately optimize sensor and FE-chip for very high radiation environment
- Copes with high hit-rates
- Interconnection needed to connect each pixel in the sensor to a readout cell in the ASIC → fine pitch bump bonding
- Thick detector modules (X_0 1.14-2.7%)
- Hybrid Pixel detectors at pp colliders due to high radiation/hit rate

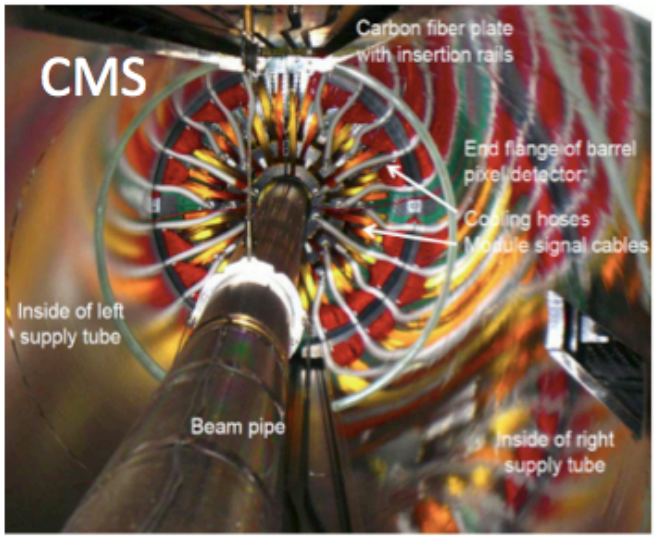


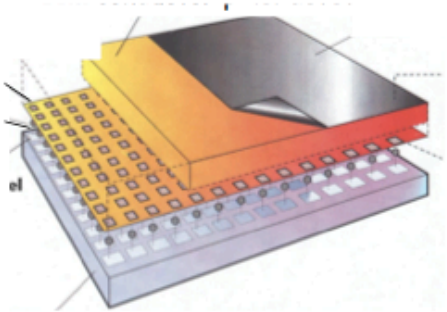


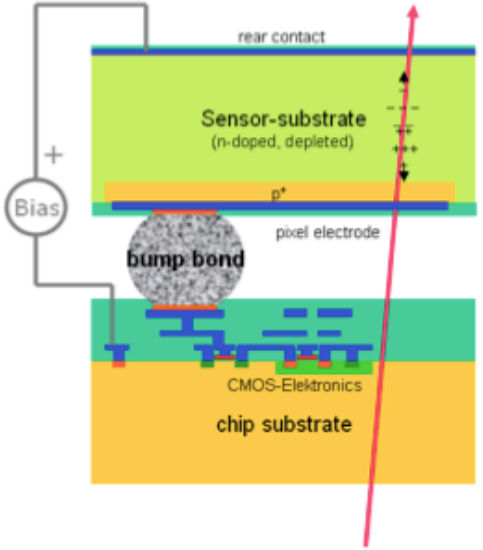
LHC Hybrid Pixel Detectors



all based on
"Hybrid Pixels"



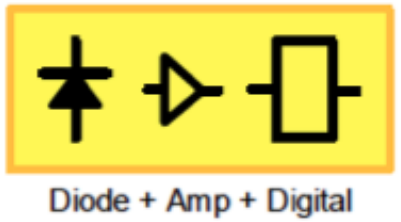


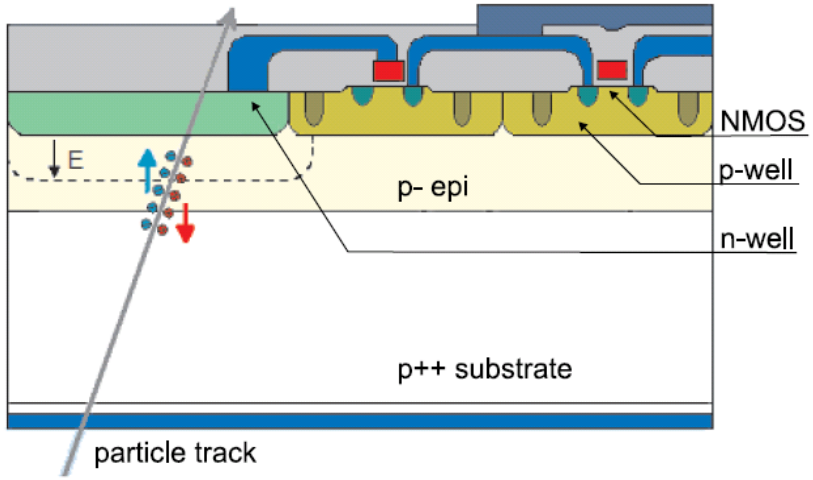


- amplification by a dedicated R/O chip
- 1-1 cell correspondence

Monolithic Active Pixel Detectors (MAPS)

- Charge generation volume integrated into the ASIC, but many different variants!
- Thin monolithic **CMOS sensor**, on-chip digital readout architecture
- Advantages for larger surfaces due to assembly simplification and costs
- Small pixel and thin detectors (e.g. 28x28 μm^2 & 0.3%/layer in Alice ITS)
- Design limits for highest hit rates
- Radiation hardness limits
- Monolithic CMOS sensors so far usually target “low-radiation environments”





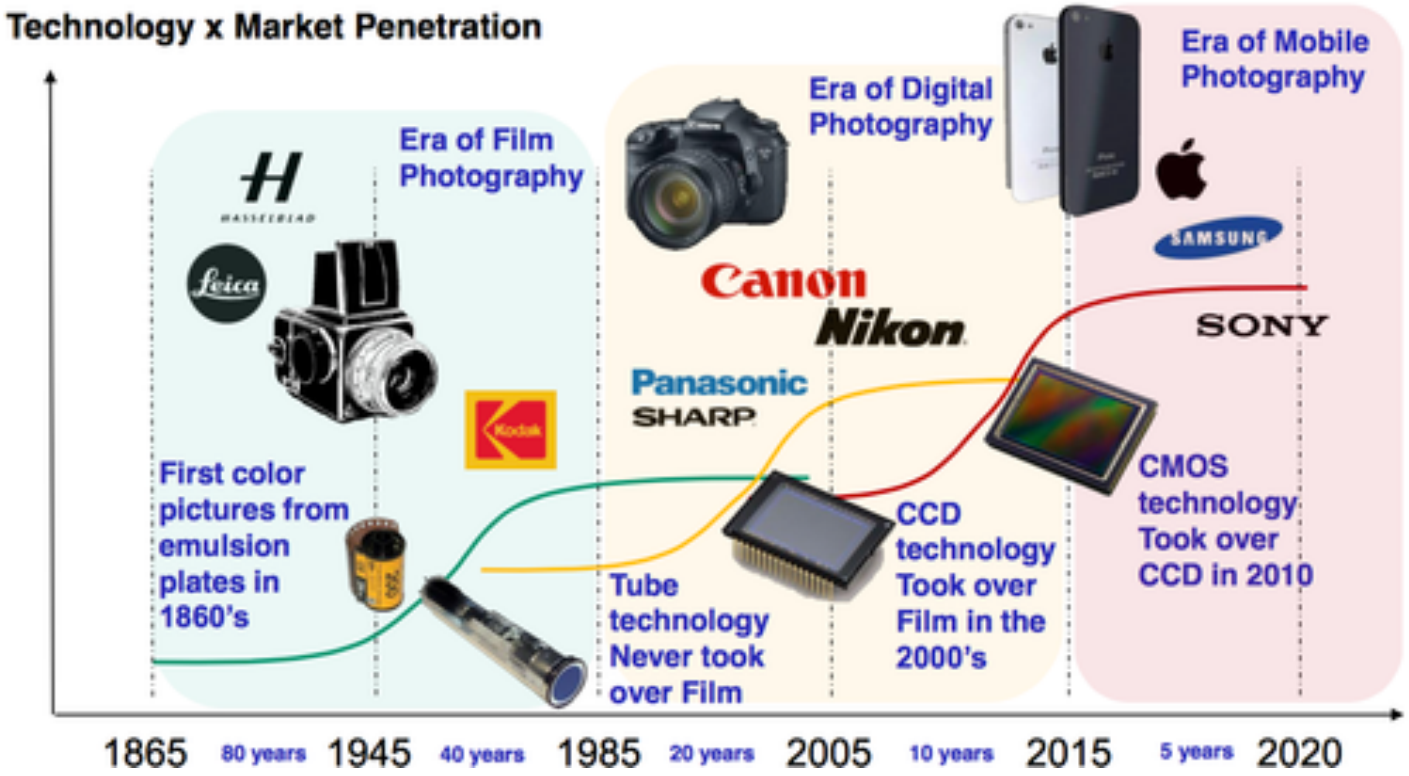
CMOS Active Image Pixel Sensors

- CMOS active image pixel sensor originally developed by NASA/JPL (patents by Caltech) in 1992
- Used (vanilla) CMOS process available at many foundries → easily accessible
- First versions contained in-pixel source follower amplifier for charge gain, low noise Correlated Double Sampling, basis for camera-on-chip
- Though specialized fab processes are required, the market has driven developments leading to CMOS sensors dominating the field.

ER Fossum, CMOS Active Pixel Sensors – Past, Present and Future, 2008
https://pdfs.semanticscholar.org/6d85/af67a846d13b7e7502f7fa96c0729c972590.pdf

CMOS Active Image Pixel Sensors

- While 1980s were dominated by CCDs (camcorder market)
- The 1990s/2000s have shown an increasing demand for CMOS imaging sensors due to the camera phone market



http://www.eetimes.com/document.asp?doc_id=1325655&image_number=1

CMOS Active Image Pixel Sensors

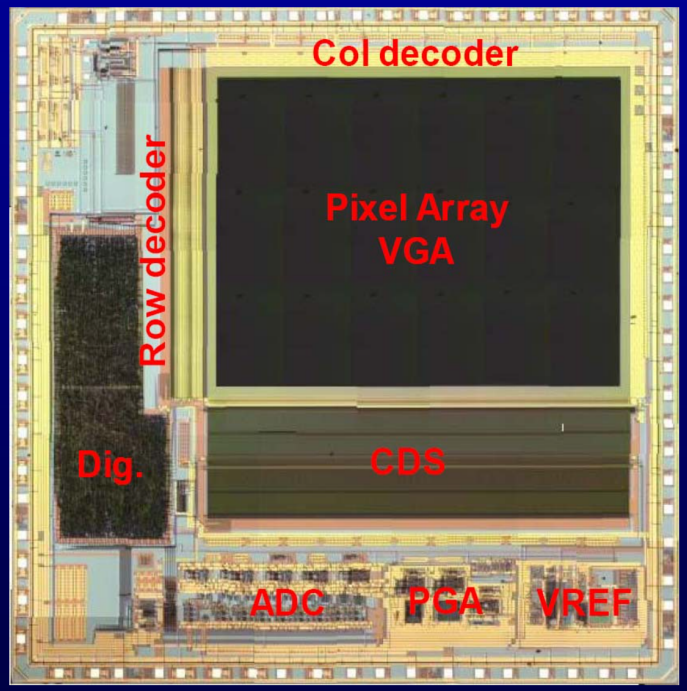
What are the advantages of CMOS imaging sensors (camera-on-chip) in industry? For example:

- Low power, important for portable devices
- Compact cameras due to system-on-a-chip
- Fewer components needed

ER Fossum, CMOS Active Pixel Sensors – Past, Present and Future, 2008
https://pdfs.semanticscholar.org/6d85/af67a846d13b7e7502f7fa96c0729c972590.pdf

Camera-on-a-chip

- Pixel array
- Signal chain
- ADC
- Digital logic
  - I/O interface
  - Timing and control
  - Exposure control
  - Color processing
- Ancillary circuits



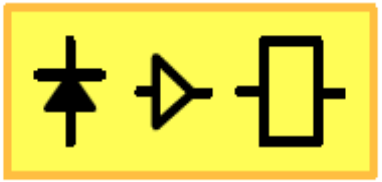
Pain et al. 2007 IISW

MAPS in HEP?

Silicon trackers are part of the core tracking systems of all present LHC experiments.

Monolithic pixel detectors can offer a number of interesting advantages for HEP experiments:

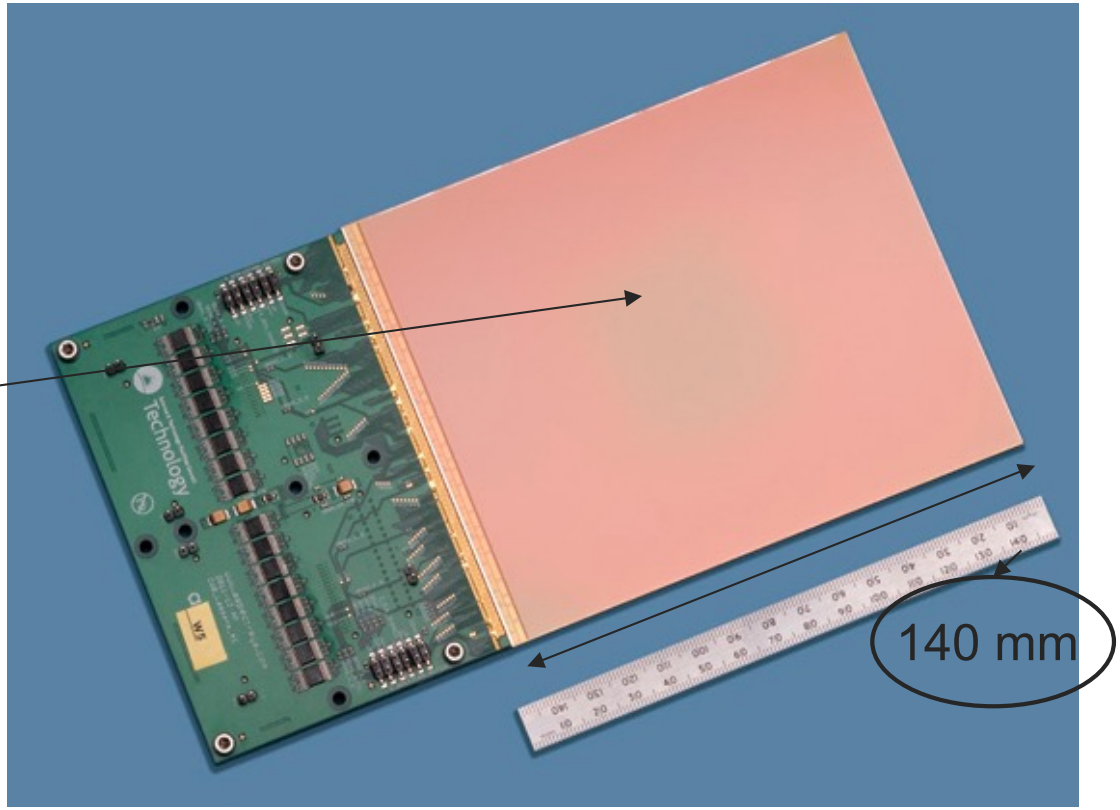
- Commercial process (8” or 12” wafers)
- Multiple vendors
- Potentially cheaper interconnection processes available
- Thin sensor (50-100 um) have less material and reduce cluster size at large eta
- ..



MAPS for Imaging and More

Many developments in the field of CMOS imaging sensors and MAPS in general within the community!

Example:
Wafers scale (8”) imaging sensor developed by the RAL team (stitched)

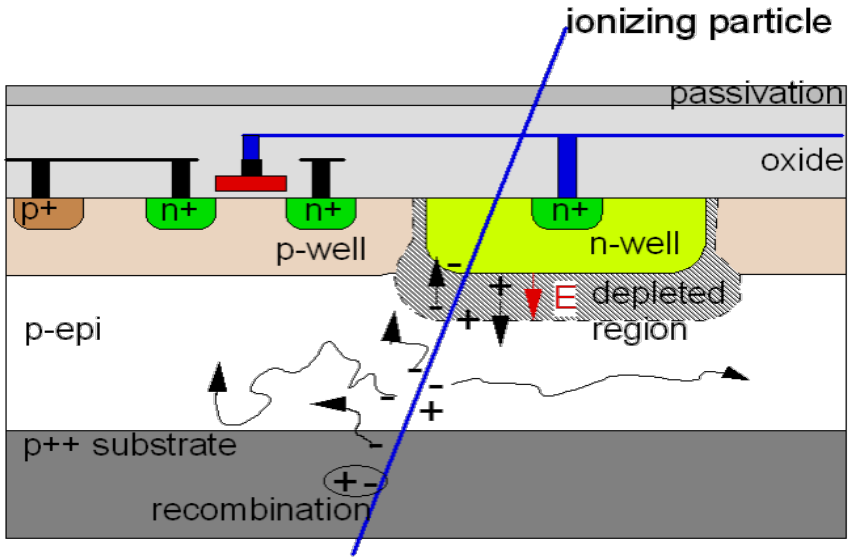


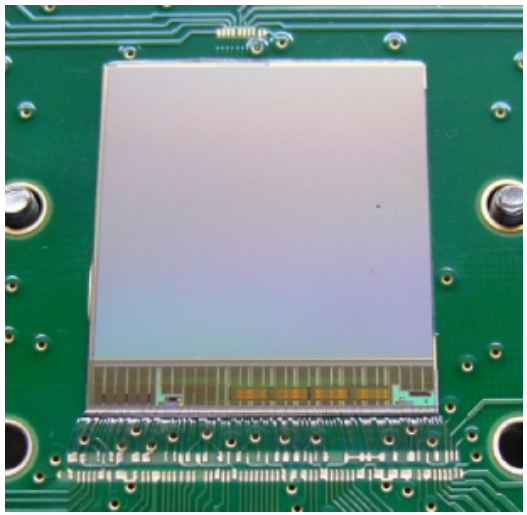
N. Guerrini, RAL, 5th school on detectors, Legnaro, April 2013

MAPS

Developments lead by IPHC created a number of monolithic pixel sensors of the MIMOSA family:

- Epitaxial wafers with collection diode and few transistors per cell (size ~ 20 x 20 μm^2), limited to NMOS transistors
- 0.35 µm CMOS technology with only one type of transistor
- Rolling shutter architecture (readout time O(100 µs))
- Charge collection mostly by diffusion
- Limited radiation tolerance (< 10^{13} n_{eq} cm^{-2})

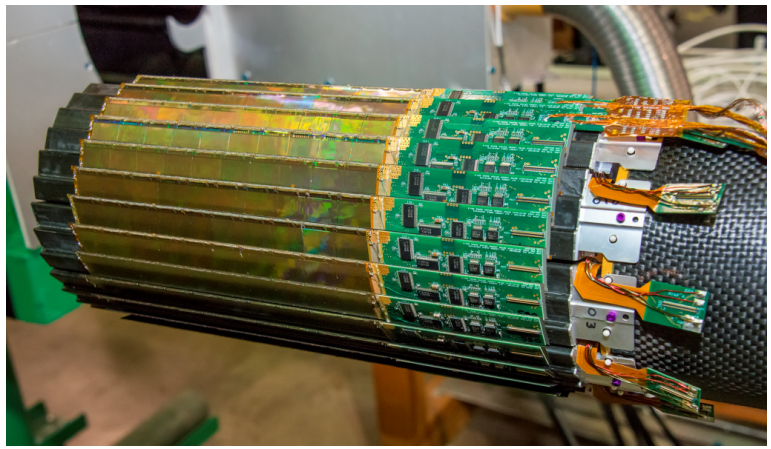




ULTIMATE chip for STAR HFT (IPHC Strasbourg)

STAR Heavy Flavour Tracker

The upgrade of the STAR HFT included also the installation of the **first MAPS based vertex tracker at a collider experiment.**



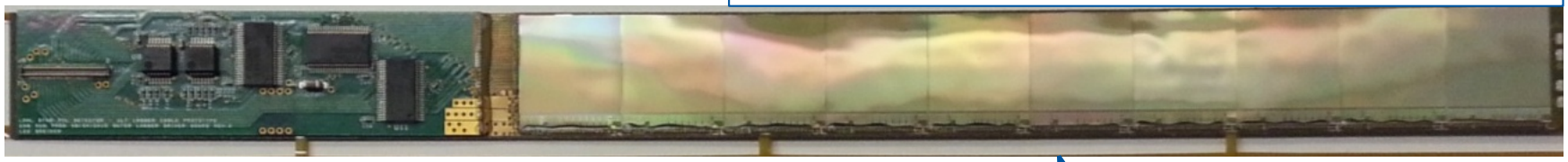
DCA Pointing resolution	(10 ⊕ 24 GeV/p·c) μm
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 μm (6 μm geometric)
Position stability	5 μm rms (20 μm envelope)
Material budget first layer	X/X_0 = 0.39% (Al cond. cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2*10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	< 1 day

After R&D and prototyping the construction of 3 trackers started in 2013.

STAR HFT

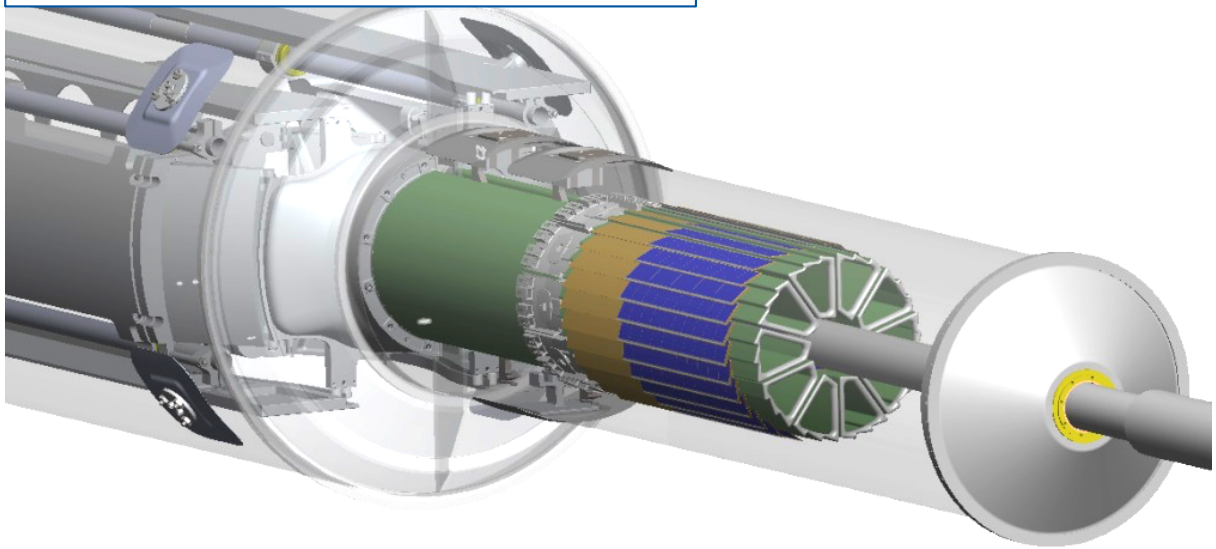
Basic Detector Element

Ladder with 10 MAPS sensors (~ 2×2 cm each)



10 sensors / ladder
4 ladders / sector
5 sectors / half
10 sectors total

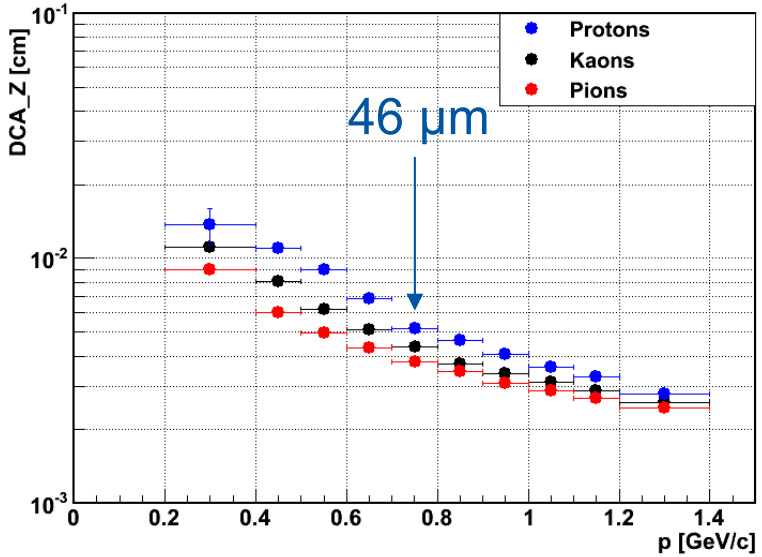
Mechanical support with kinematic mounts (insertion side)



carbon fiber sector tubes (~ 200 µm thick)

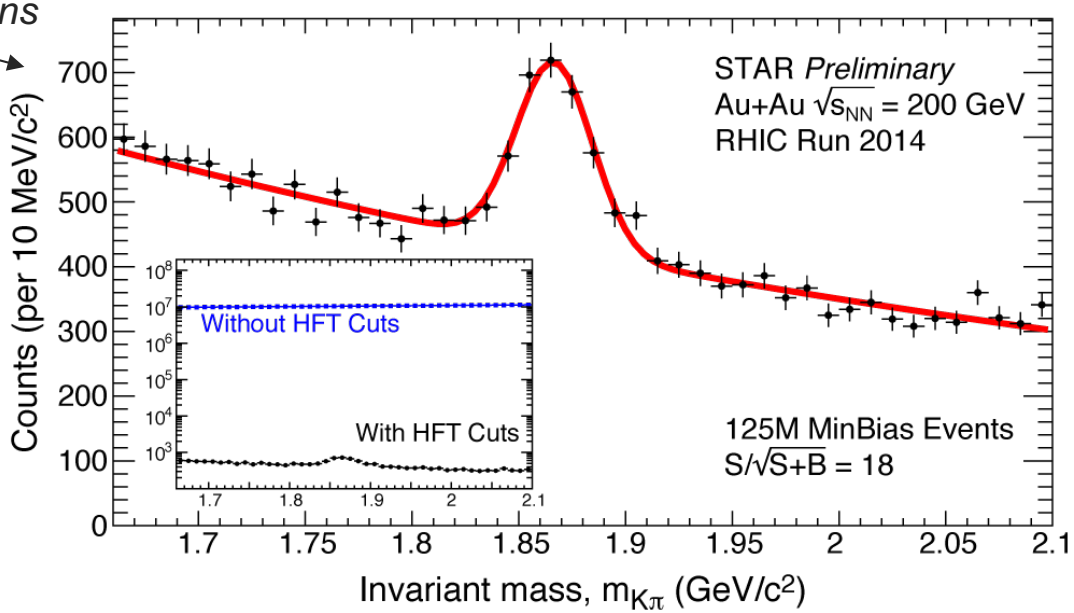
STAR HFT

- DCA pointing resolution
  - Design requirement exceeded: 46 µm for 750 MeV/c Kaons for the **2 sectors** equipped **with aluminum cables on inner layer**
  - ~ 30 µm for p > 1 GeV/c
  - From 2015: all sectors equipped with aluminum cables on the inner layer



$D^0 \rightarrow K\,\pi$ production *in* $\sqrt{s_{NN}}$ **=** *200GeV Au+Au collisions (partial event sample)*

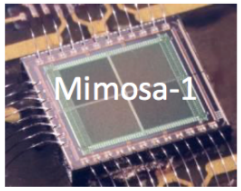
- Physics of D-meson productions
  - High significance signal
  - Nuclear modification factor R_{AA}
  - Collective flow v_2
- First Λ_c^+ signal observed in HI collisions (QM 2017)!

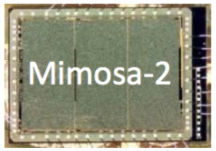


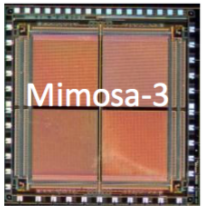
MAPS Evolution

L. Musa, 30 years HI Forum
November 2016

Owing to the industrial development of CMOS imaging sensors and the intensive R&D work (IPHC, RAL, CERN)







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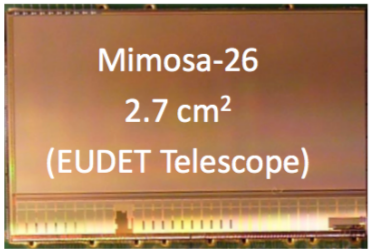
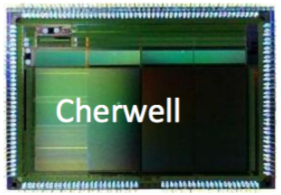
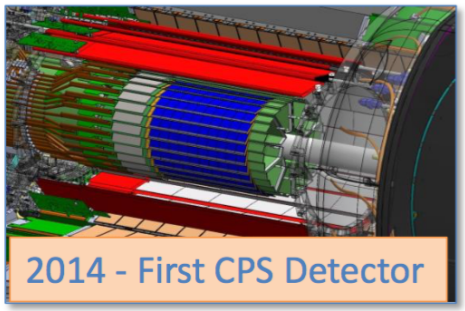
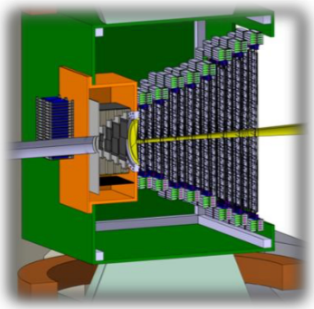




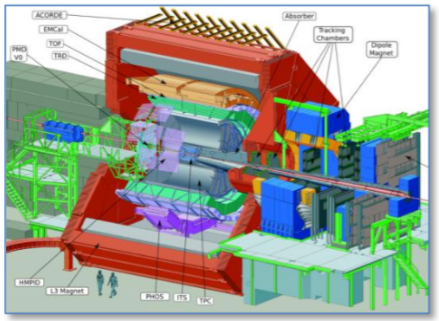
... several HI experiments have selected CMOS pixel sensors for their inner trackers



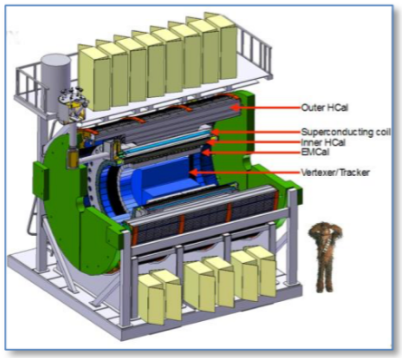
STAR HFT
0.16 m² – 356 M pixels



CBM MVD
0.08 m² – 146 M pixel



ALICE ITS Upgrade (and MFT)
10 m² – 12 G pixel



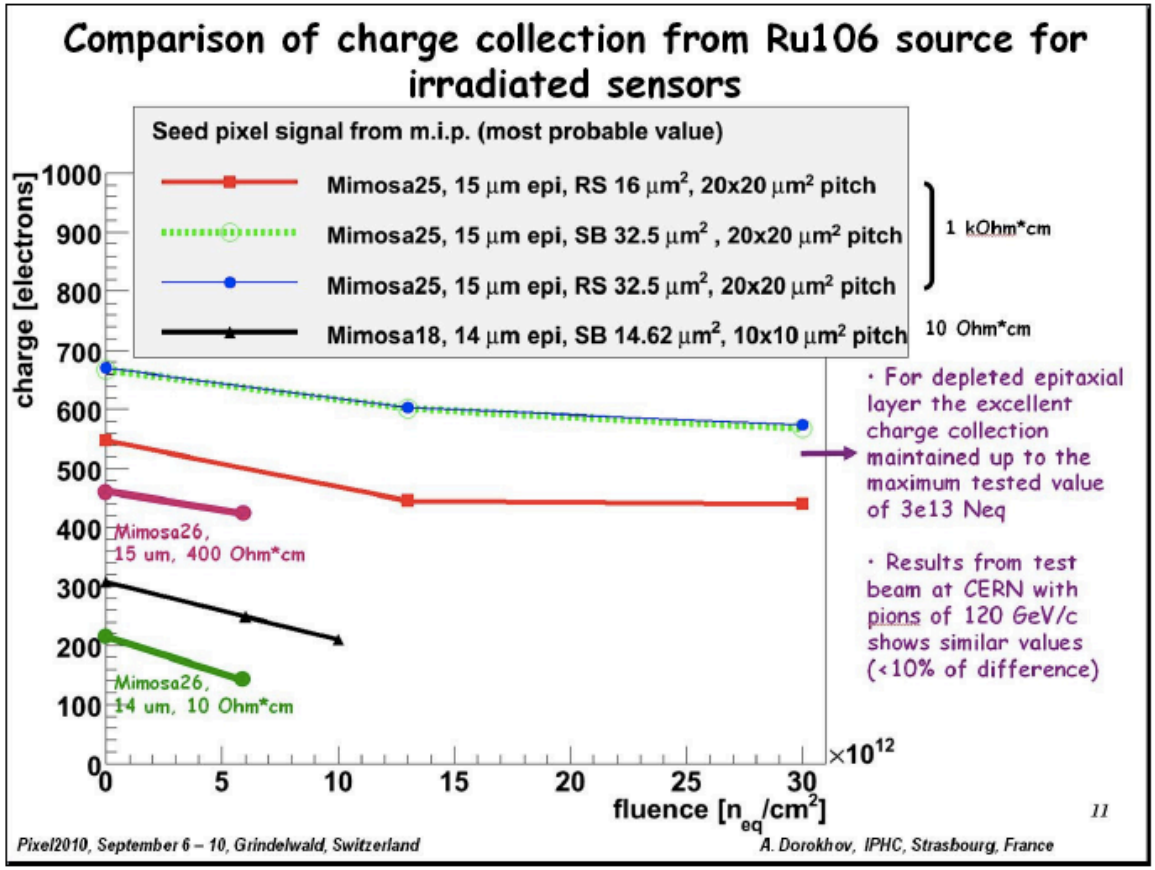
sPHENIX
0.2 m² – 251 M pixel

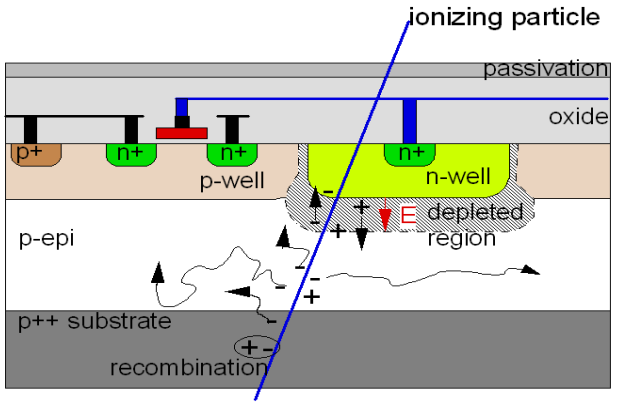
30

Radiation Tolerance

Transistor radiation tolerance comes “for free” for deep sub micron processes and improved design layout.

Charge collection by diffusion suffers from radiation damage beyond 10^{13} n_{eq} cm^{-2}!





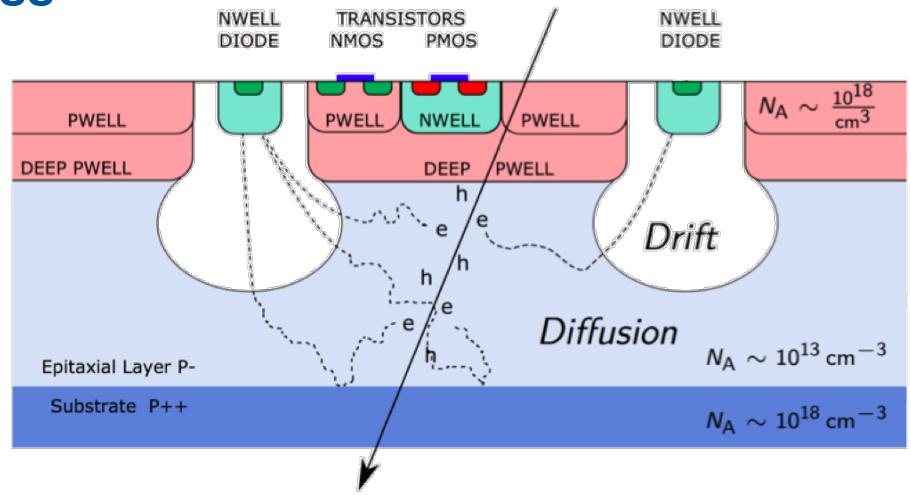
Deplete part or all of the charge generation volume to **collect charge by drift**

A. Dorokhov et al., Pixel 2010

MAPS

TowerJazz 0.18µm CMOS imaging process

- N-well collection electrode in high resistivity epitaxial layer (>1kOhmcm)
- Present state-of-art based on quadruple well allows full CMOS
- High resistivity (> 1kΩ cm) epi-layer (p-type, 20-40 µm thick) on p-substrate
- Moderate reverse bias => increase depletion region around Nwell collection diode to collect more charges by drift



Process chosen for the ALICE ITS (Inner Tracking System) Upgrade

ALICE Inner Tracking System Upgrade

Based on high resistivity epi layer MAPS

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

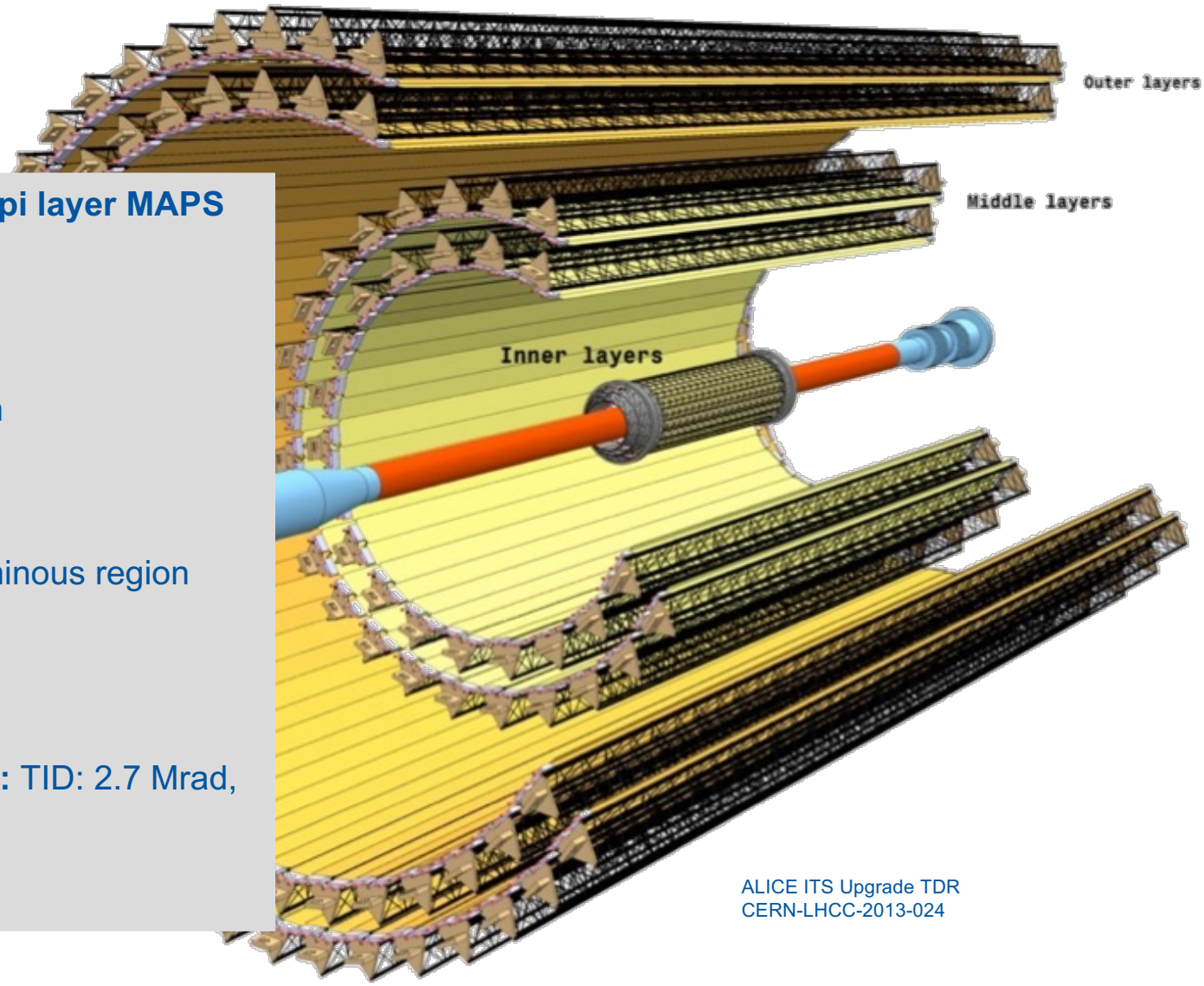
~ 10 m^2

$|\eta|<1.22$ over 90% of the luminous region

0.3% X_0/layer (IB)
0.8 % X_0/layer (OB)

Radiation level (IB, layer 0): TID: 2.7 Mrad, 1.7 x 10^{13} 1 MeV n_{eq} cm^{-2}

Installation during LS2



ALICE ITS Upgrade TDR
CERN-LHCC-2013-024

ALICE ITS Upgrade Design Requirements

Improve impact parameter resolution by factor of ~3 in (r-ϕ) and ~5 in (z)

- Get closer to IP: 39 mm → 21 mm (layer 0)
- Reduce beampipe radius: 29 mm → 18.2 mm
- Reduce material budget: 1.14 % X_0 → 0.3 % X_0 (inner layers)
- Reduce pixel size: (50 µm x 425 µm) → O(30 µm x 30 µm)

High standalone tracking efficiency and p_T resolution

- Increase granularity and radial extension → 7 pixel layers

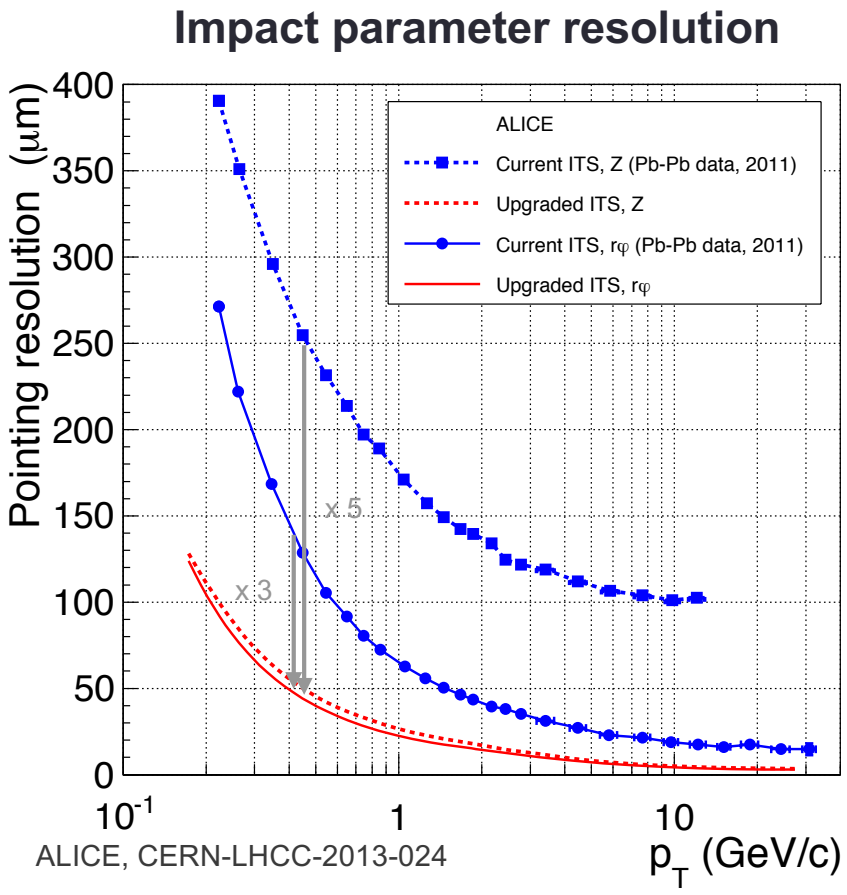
Fast readout

- Readout of Pb-Pb interactions at 50 kHz (presently 1kHz) and 400 kHz in p-p interactions

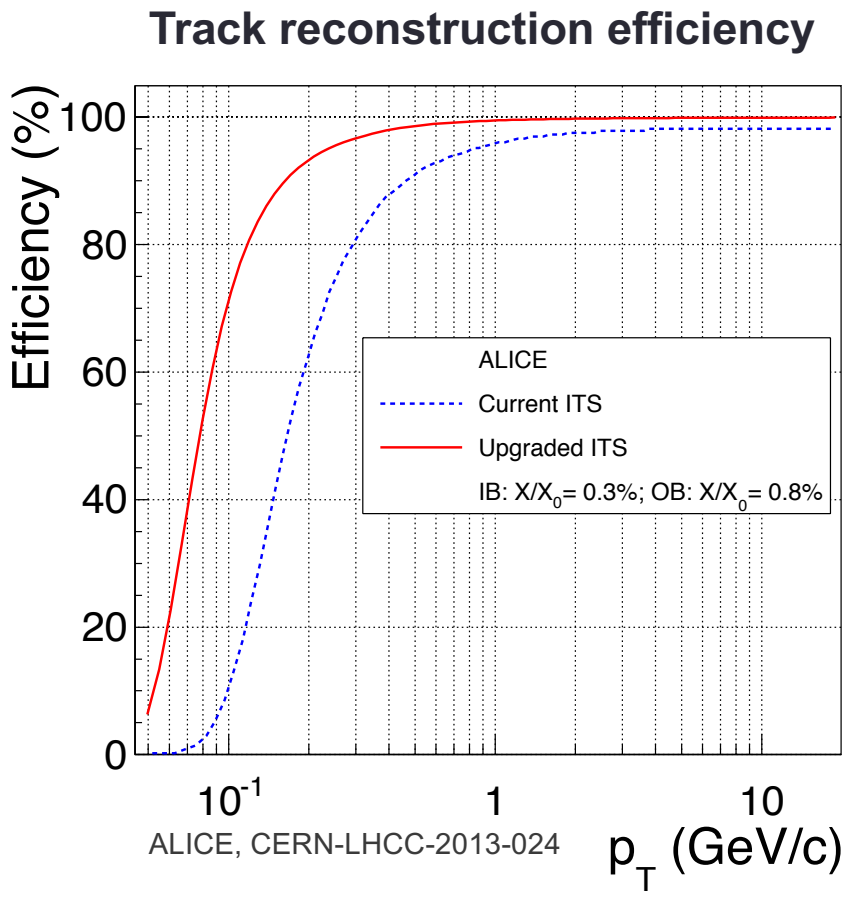
Fast insertion/removal for yearly maintenance

- Possibility to replace non functioning detector modules during yearly shutdown

ALICE ITS Upgrade Tracking Performance



Improved impact parameter resolution

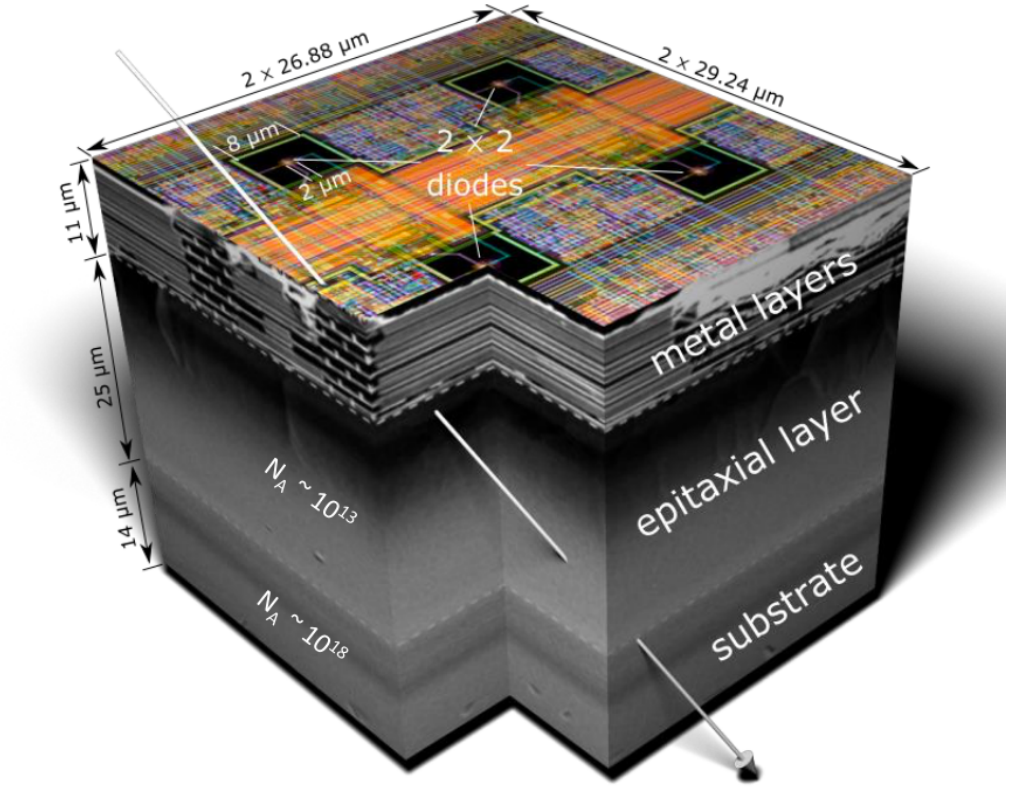


High standalone tracking efficiency

ALICE ITS Pixel Technology

TowerJazz 0.18 µm CMOS imaging process

- High resistivity wafers (>1kOhmcm) with 25 µm p-type epitaxial layer on p-substrate
- Small n-well diode (2 µm diameter), ~ 100 times smaller than pixel size (~27 x 29 µm^2)
- Reverse bias voltage applied to increase the depleted region around the collection diode
- Deep p-well shields the n-well of the PMOS transistors (→full CMOS)



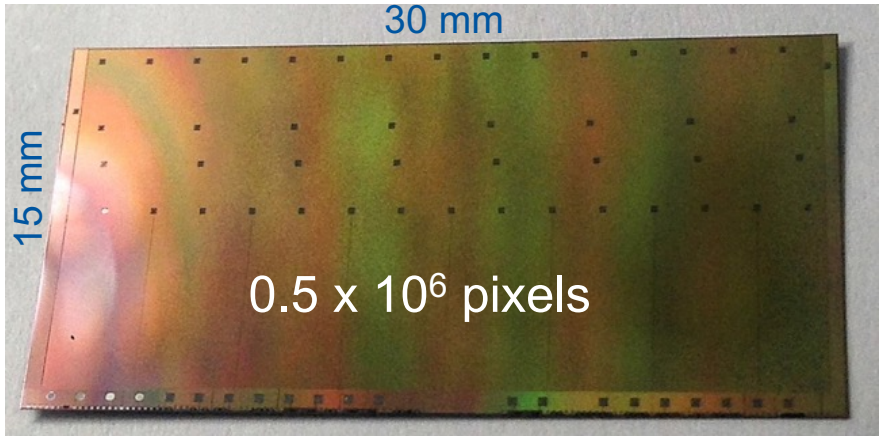
Chip Development

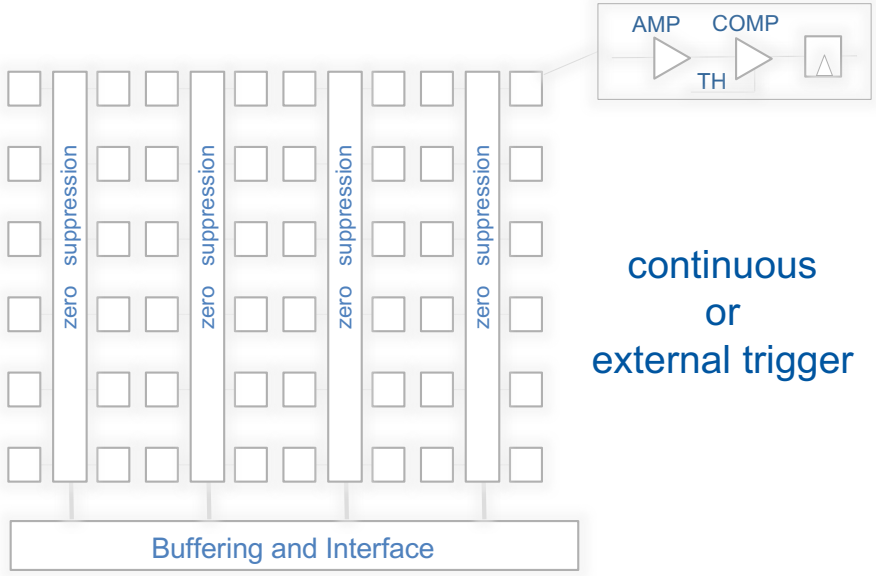
Design team from CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC

2012	Explorer	20 µm x 20 µm and 30 x 30 µm pixels (analogue readout) 1.8 x 1.8 mm^2, study of pixel geometry, starting material, radiation
2013	pALPIDEss-0	Matrix with 64 columns x 512 rows, 22 µm x 22 µm pixels, 11 x 1.8 mm^2, in-pixel discrimination and buffering, zero suppression
2014	pALPIDE-1	**First full scale prototype!** 28 µm x 28 µm pixels, 15 x 30 mm^2, four sectors with variants, 1 register/pixel, no final interface
8/2015	pALPIDE-2	**Full scale prototype,** four sectors with variants, optimisation of circuits, integration in modules, no high speed serial output
10/2015	pALPIDE-3	**Full scale prototype,** eight sectors with variants, all communincation features, no ADC, no temperature sensor)
8/2016	ALPIDE	**Final chip**

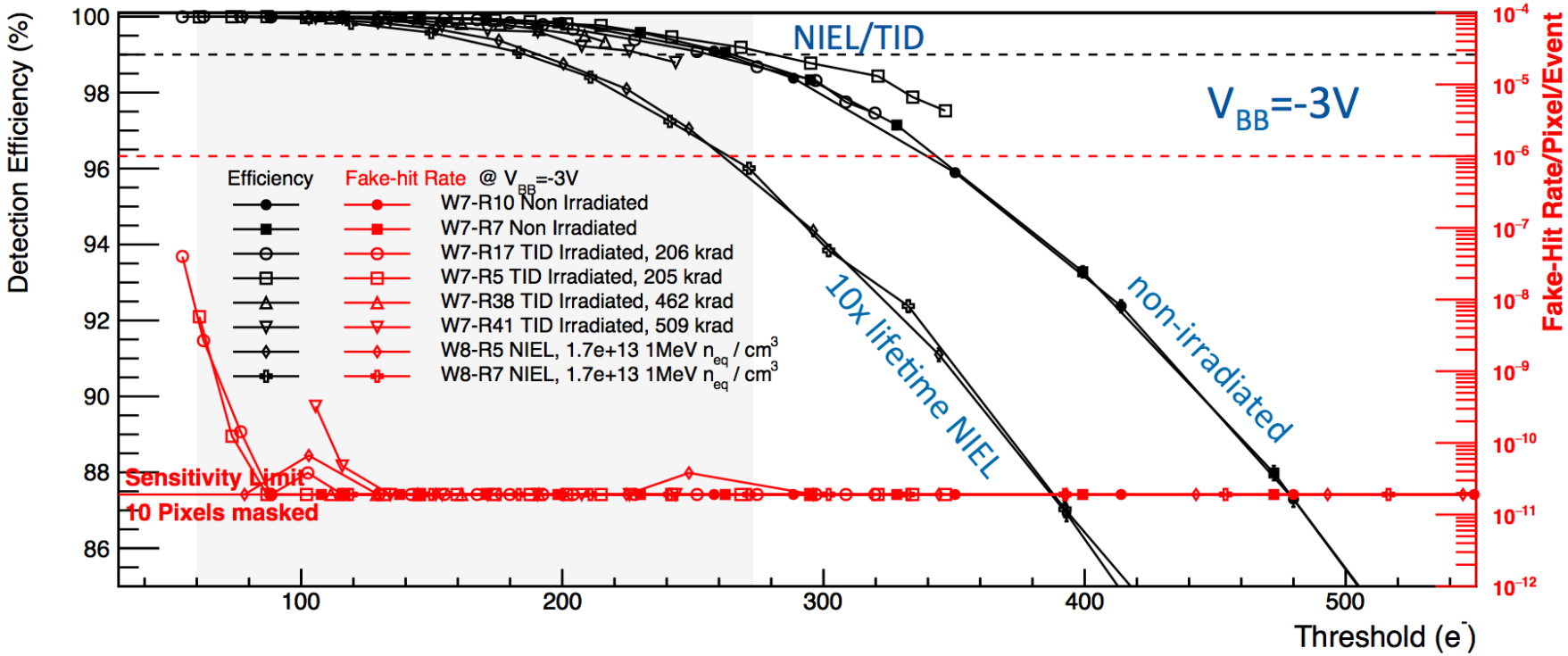
ALPIDE Chip

- Pixel size: 29 x 27 μm^2 with low power front-end (40 nW)
- Asynchronous sparsified digital readout
- **Power density ~300 nW/pixel**
- Minimized inactive area on the edge due to pads-over-matrix design (~ 1.1 x 30 mm^2)
- Full size prototypes produced on different epitaxial wafers
- **Partial depletion of the sensitive region due to back bias**
- Extensive tests before and after irradiation



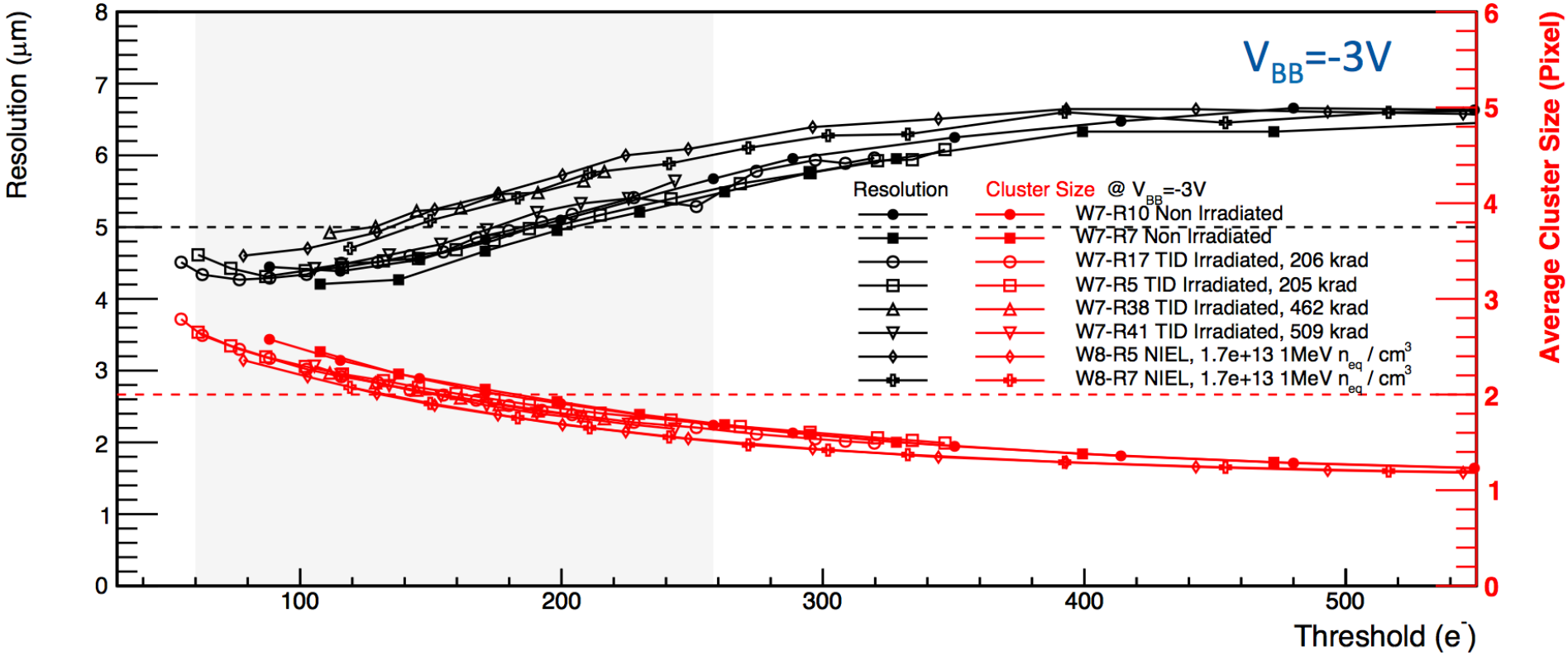


ALPIDE Chip Performance



- Large operational margin before and after irradiation up to 10 x lifetime NIEL
- Chip-to-chip fluctuations negligible
- Fake hit rate << 10^{-5}

ALPIDE Chip Performance

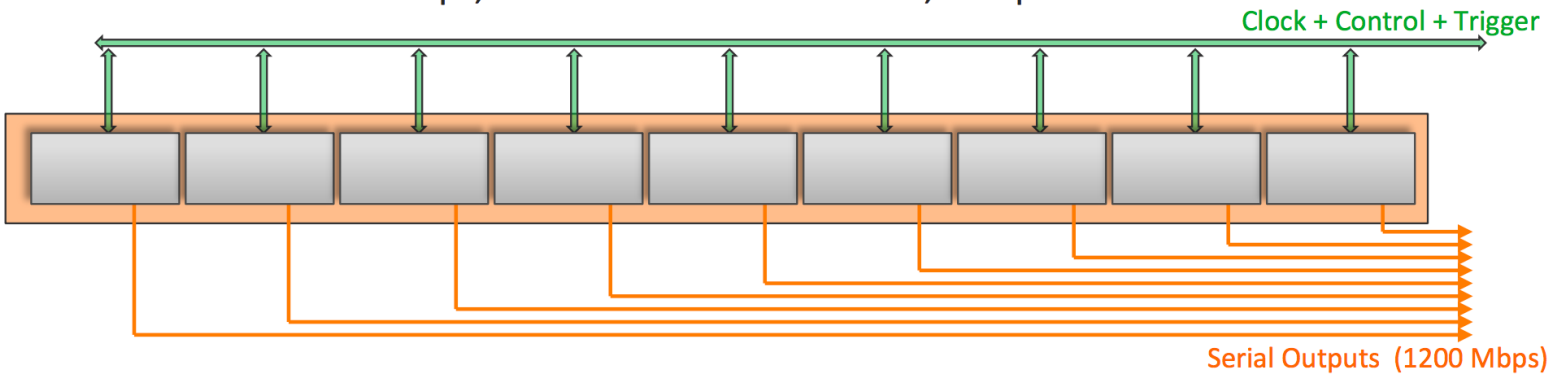


- Similar performance before and after irradiation
- Chip-to-chip fluctuations negligible
- Resolution of 4-6 µm up to ~ 300 electrons threshold range

ITS Hybrid Integrated Circuits (HICs)

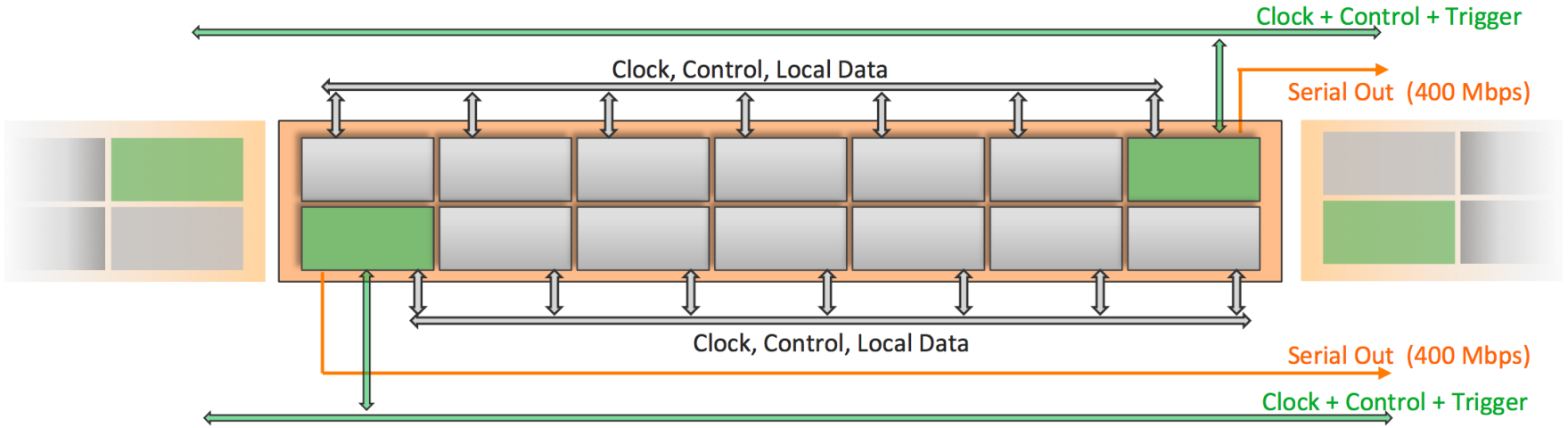
Each HIC (IB and OB) consists of X chips and a Flexible Printed Circuit (FPC):

ITS Inner Barrel Module – 9 chips, common clock and control, independent data lines



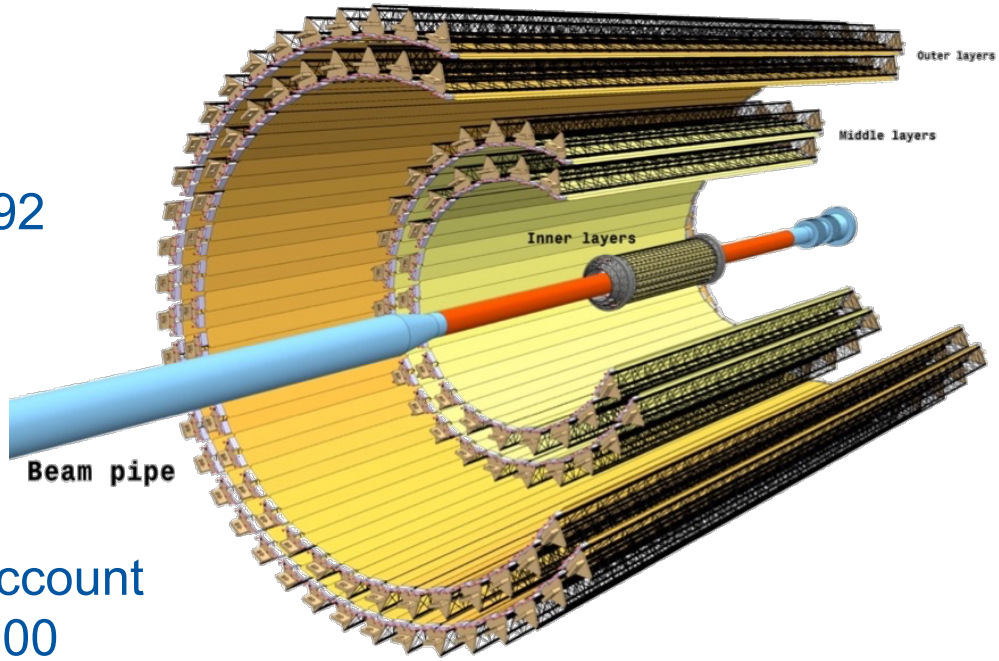
ITS Outer Barrel Module – 2 groups of chips, Master + 6 Slaves

Only the Master interfaces to the external world and bridges control and data transfer



ALICE ITS in Numbers

- Inner Barrel HICs (x 9 chips): 48
- Outer Barrel HICs (x 14 chips): 1692
- Chips IB: 432
- Chips OB: 23 688



In order to supply 20% spares and to account for yield losses at the different steps 1400 wafers with each 46 chips

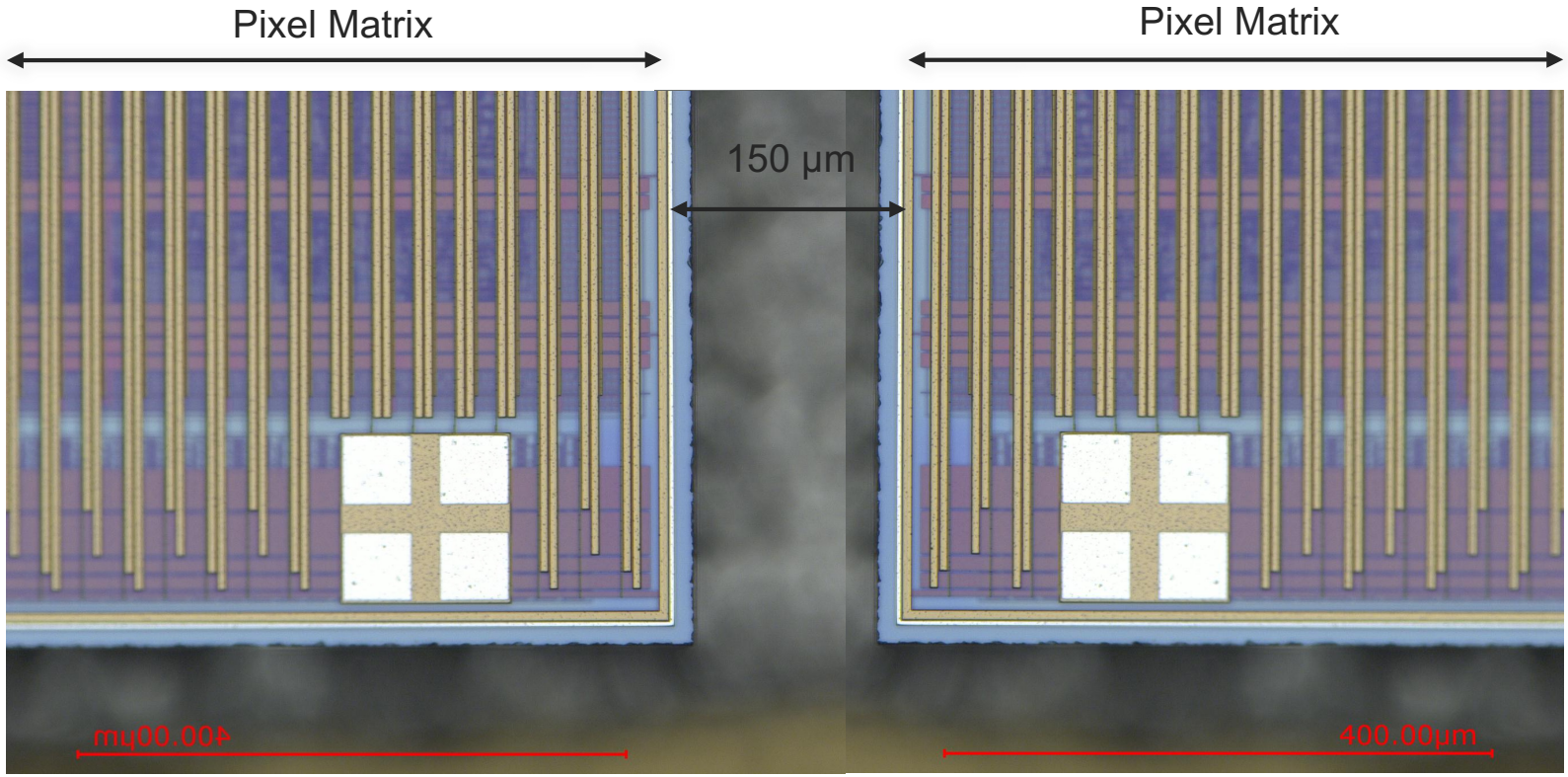
will be produced, thus resulting in

~64 000 chips

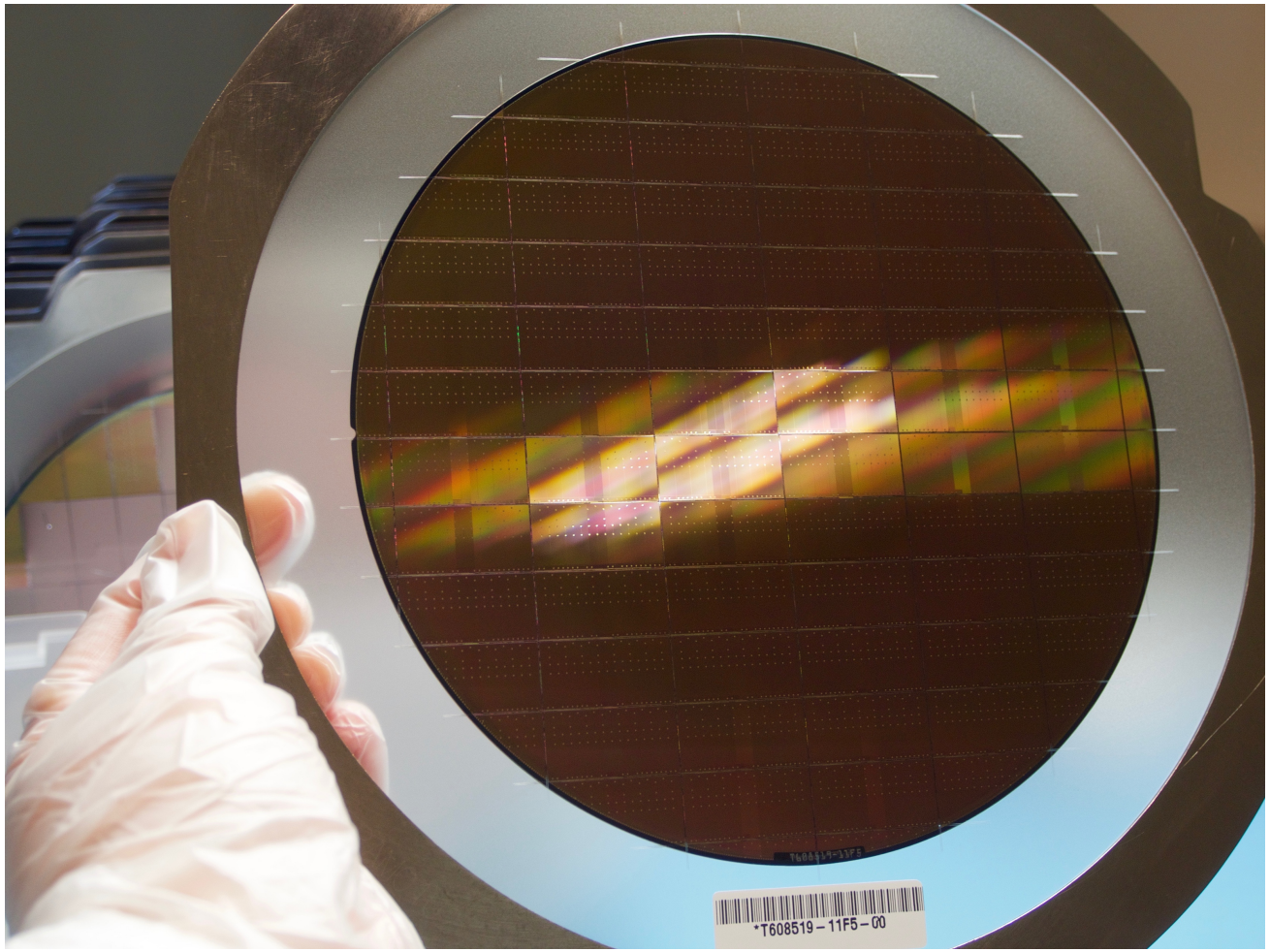
to be thinned, diced and tested.

Thinning and Dicing

- For the IB the silicon pixel chips are thinned to 50 µm, for the OB they are thinned to 100 µm.
- To minimize the dead area between chips in a module, the spacing between the active areas of two chips along z is 150 µm.



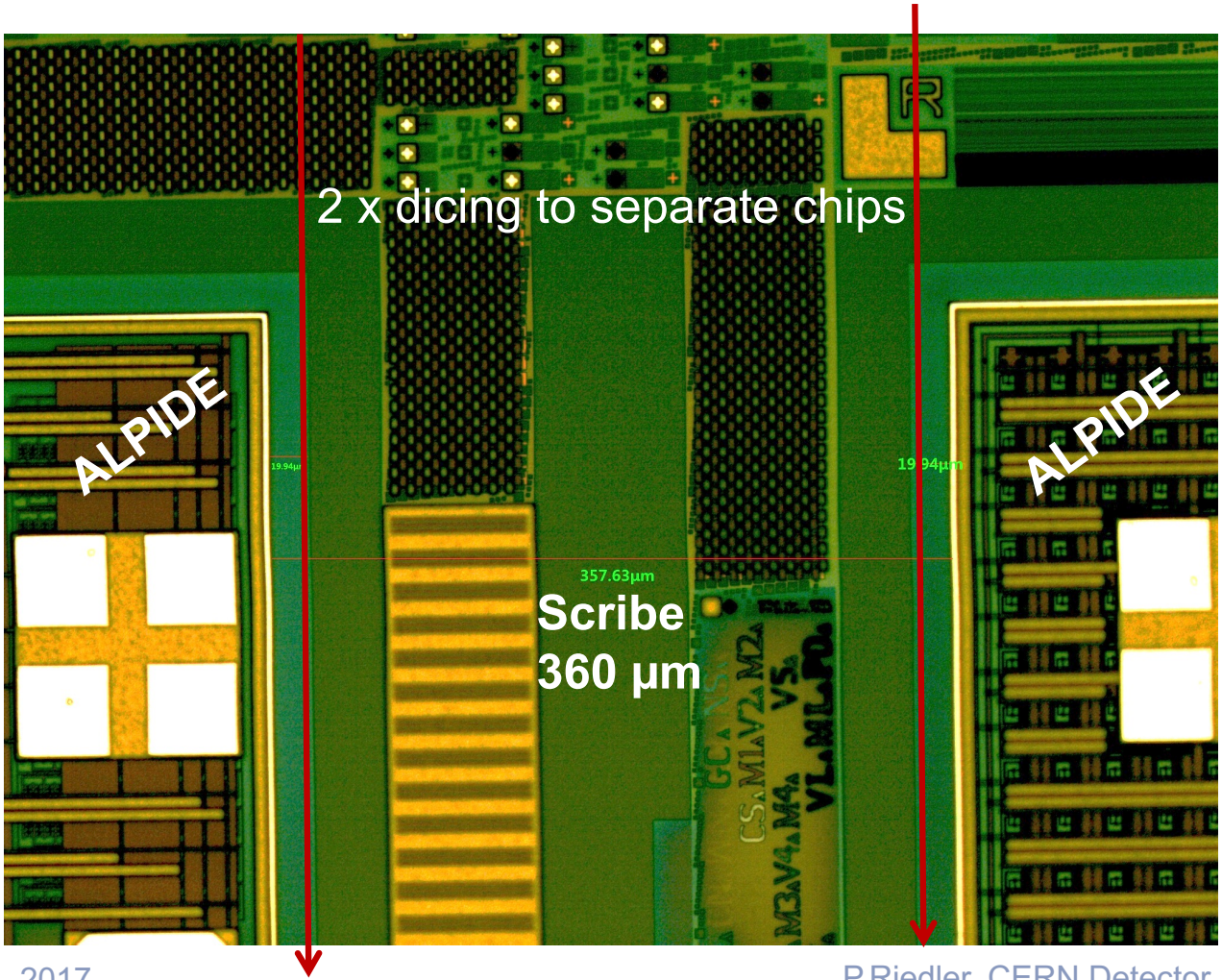
Thinned ALPIDE Wafer



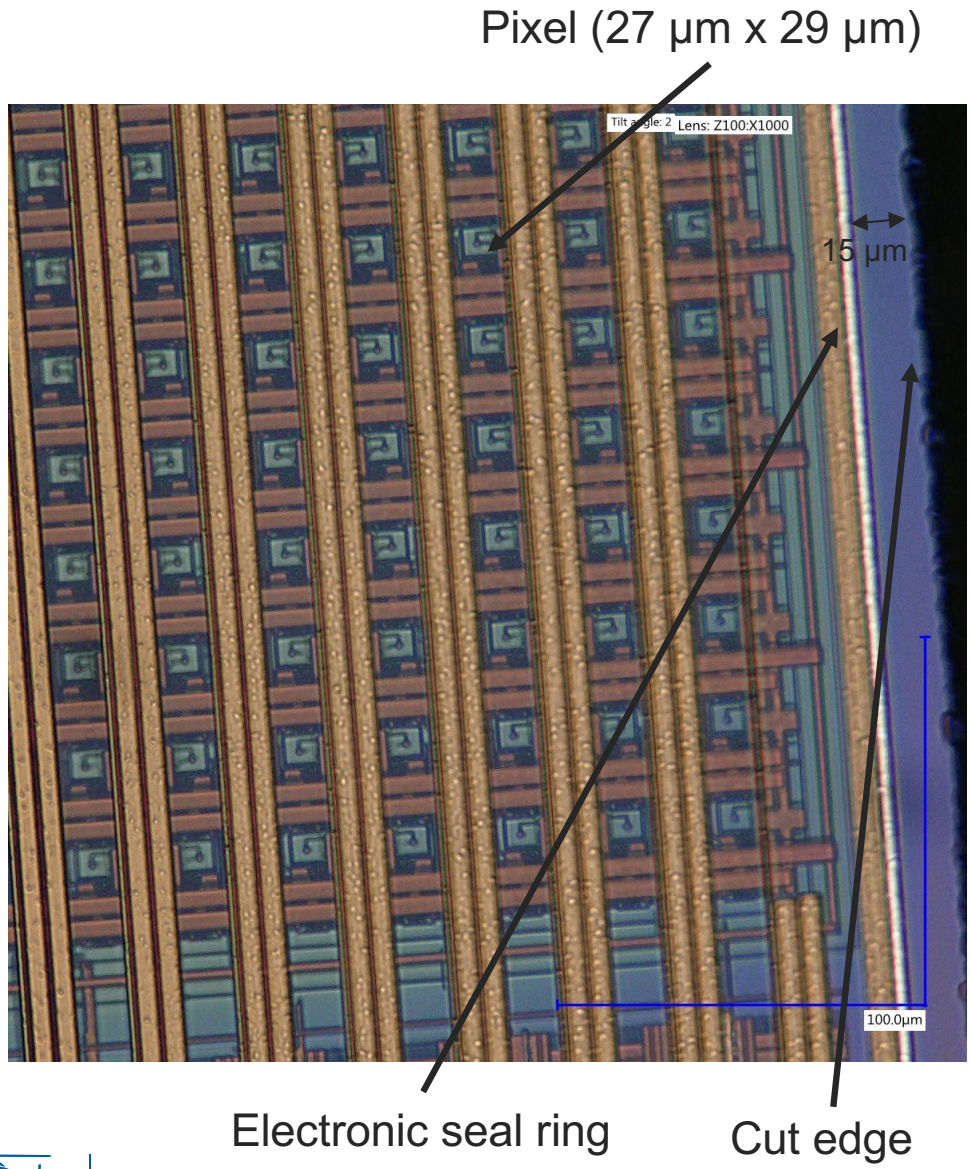
Thinning process optimised to reduce bending of the chips (<300 µm over 3 cm for 50 µm thick chips).

“Design for Dicing”

In order to have an optimum cut line at the chip edges, the reticle layout on the wafer has been adapted such to have a completely test structure free region next to the seal-ring where the blade passed through the silicon.



Dicing Requirements



Stringent requirements on the dicing, i.e. cut edge at 15 µm from the electronics seal ring (+/- 5 µm) with no chip-outs or cracks within 10 µm from the sealring.

Visual inspection of all edges prior to assembly!

“Dead space” on the chip edge ~30 µm on three edges, and about 1.1 mm on the side with pads → maximise sensitive area

Module Studies

During the R&D different (new) ways to assembly a silicon module were explored (EP-AID/ESE/DT):

Minimising the dead zone at the edge of the chip in order to achieve a maximum of sensitive surface in the detector:

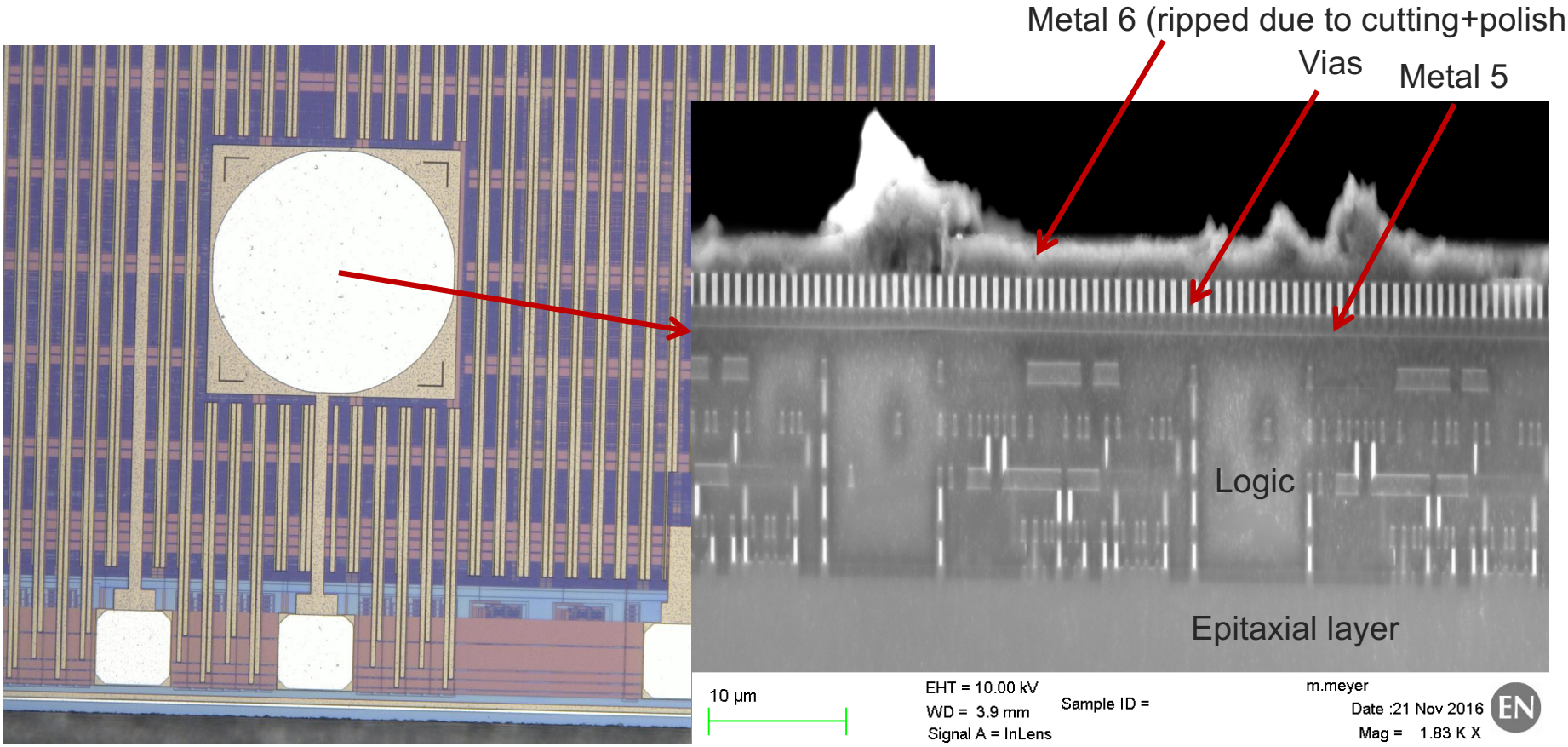
- Extending the pixel matrix as far as possible to the edge.
- Clearing the chip edges of test structures to allow dicing close to the sealring.
- Redistributing supply and I/O pads over the pixel matrix.

New interconnection techniques were studied to make the connection between the chips and a flex cable:

- Direct laser soldering
- Conductive glues

Pads over Matrix

67 pads distributed over the pixel matrix with 300 µm diameter and made of two metal layers (M5,6)

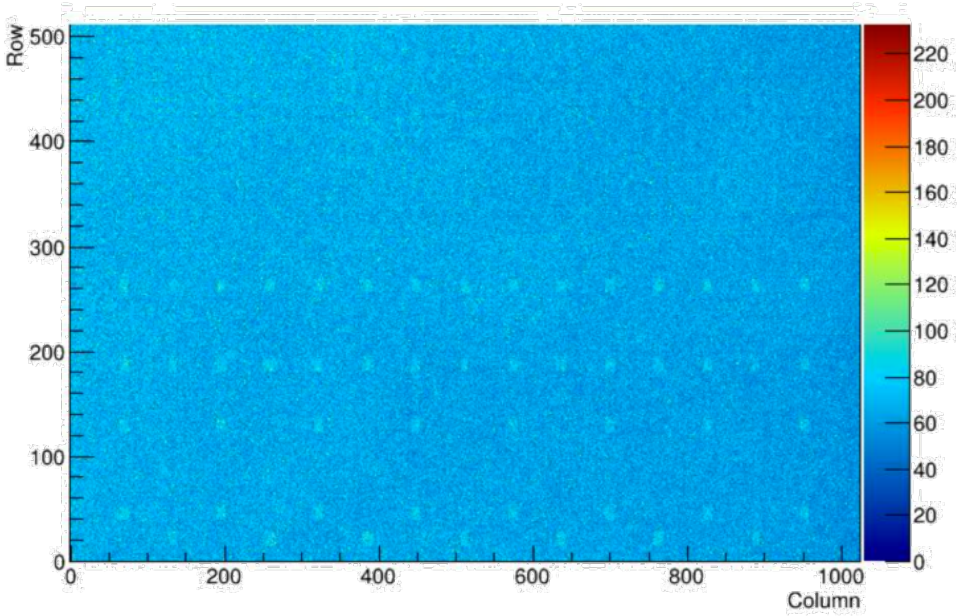


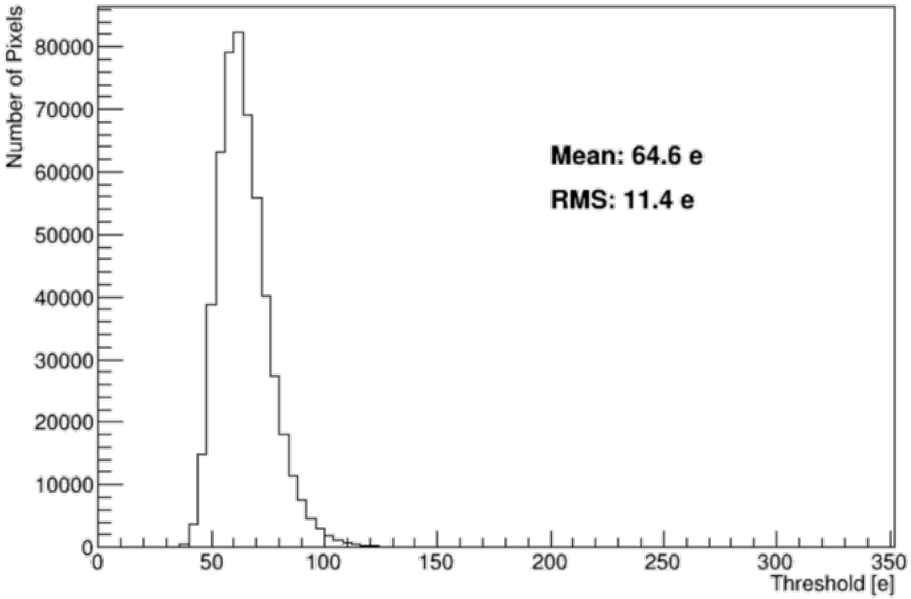
M.Meyer, EN-MME-MM

Pad over Matrix

Laboratory tests:

- Thresholds from S-curve scan show slight tail in the distribution due to pads over matrix
- No effects seen in the testbeam measurements → pads over matrix ok



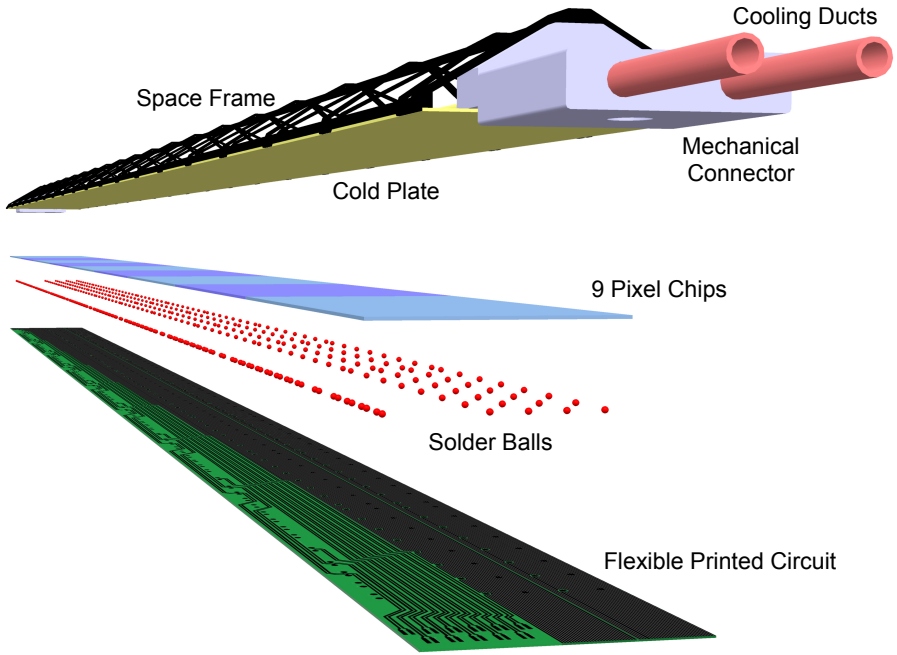


M. Keil, ALPIDE PRR, Dec.2016

Interconnection Study

Two types of interconnections for the pads over matrix to the FPC:

- **Direct laser soldering**
- **Conductive anisotropic glue** (not discussed here)

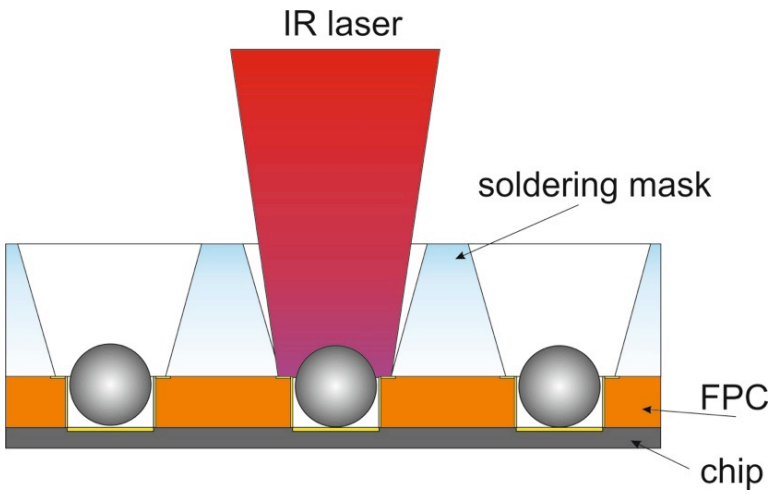


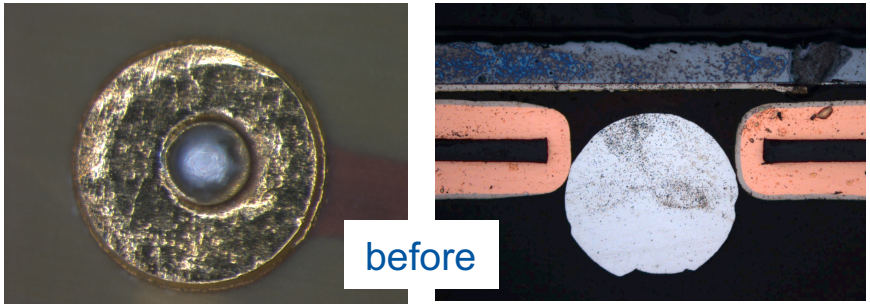
Laser soldering:

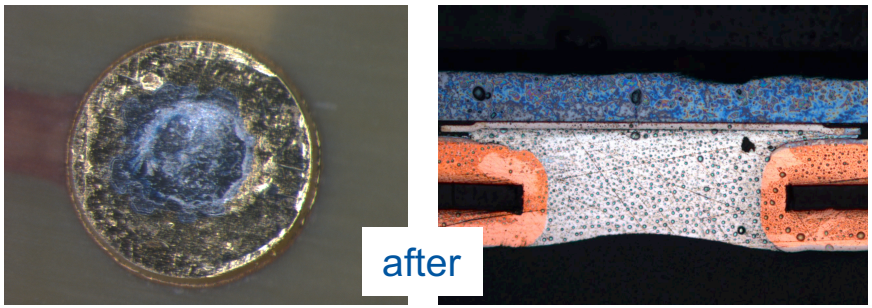
- The connection between the chip and the flex is made by a solder ball, thus providing an excellent electrical connection
- The solder connection also provides the mechanical connection to the flex

Laser Soldering

- **Industrial technique adapted for ALICE ITS studies**
- **Flux-less soldering** of ~200 µm diameter Sn/Ag(96.5/3.5) balls (227 ^{o}C melting T) in vacuum (≤10^{-1} mbar)
- **IR diode laser**, 976 nm, 25 W, 50 mm focal length, 250 mm beam spot size
- **Laser power modulated** by pyrometer, programmable T profile ensures precise limitation of heating
- **Soldering mask** (in Macor® or Rubalit ®) used to push FPC on chip and guide soldering balls inside FPC vias

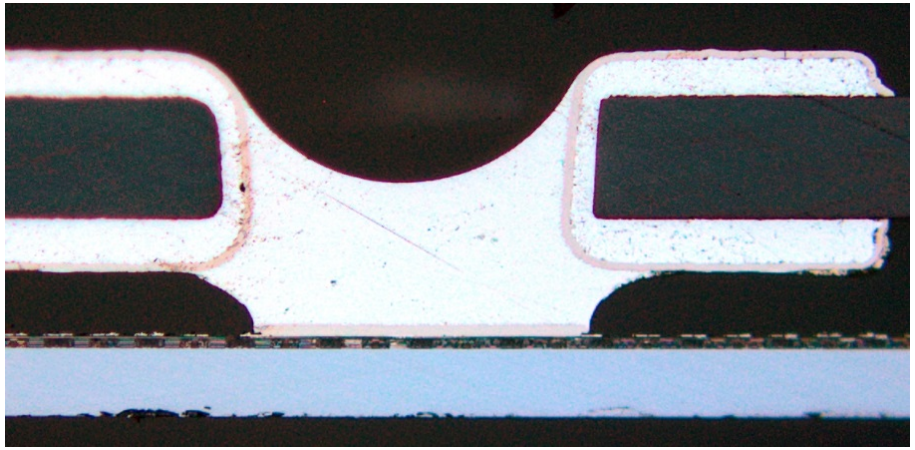




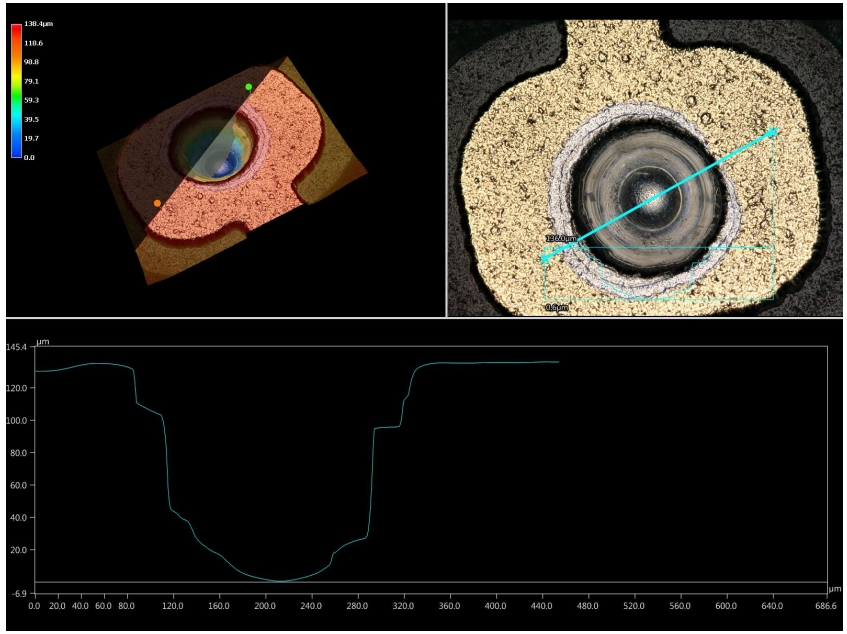


Laser Soldering

Detailed study, building single chips connected to FPCs as well as full size modules. Optimisation of the process included metallurgical and optical analysis of the solder connections.



A. Junique



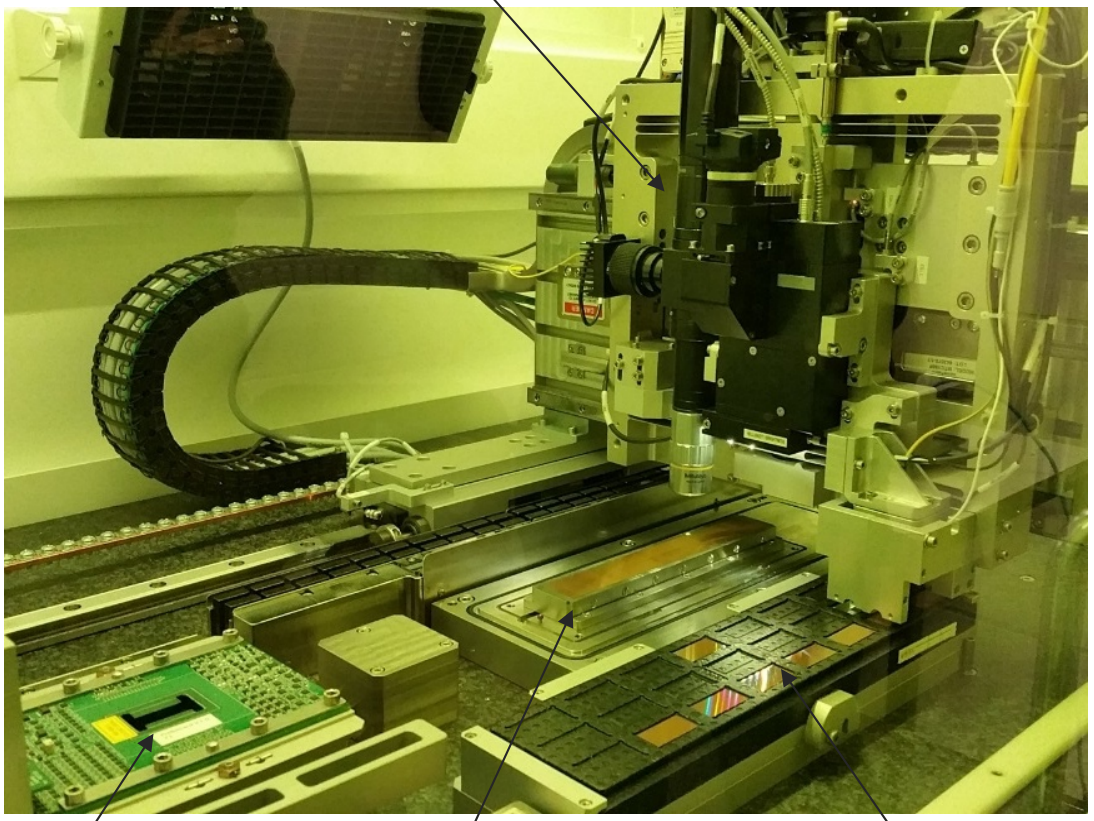
Study to achieve required 99.5% yield in soldering quality (100% for signal connections) could not be completed in the available time → **decided to use wire bonding.**

Laser soldering still needs R&D work, but is a promising option (ditto for the conductive anisotropic glue).

IB and OB HIC Production

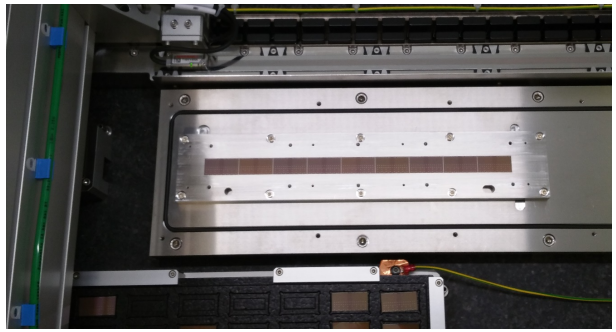
The HICs are being assembled using a custom machine (ALICIA), which aligns the chips into the HIC positions (position accuracy +/- 5 µm) and provides the possibility to probe the chips and to do a fully automatic visual inspection.

The HICs will be produced in **several construction centers:** CERN (DSF cleanroom), Bari, Liverpool (UK), Pusan (South Korea), Wuhan (China).

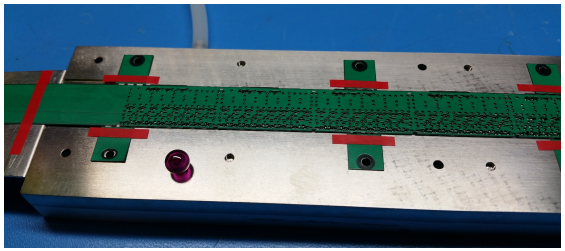


HIC Assembly (IB)

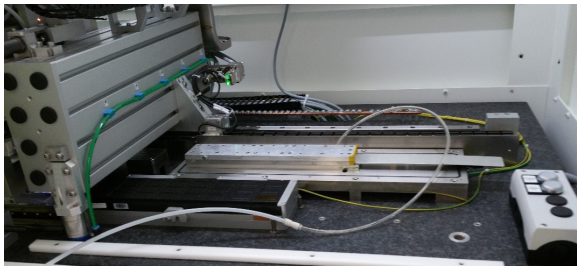
A. Di Mauro



Chip alignment

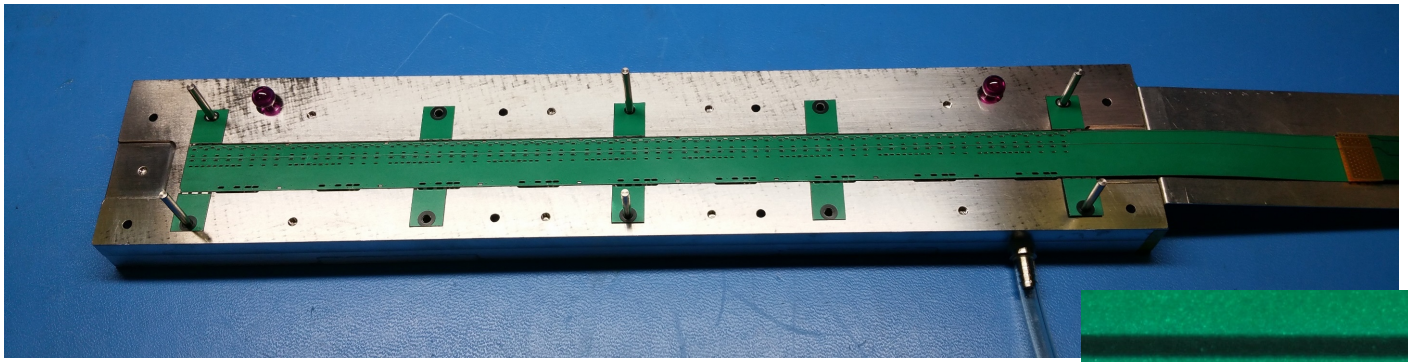


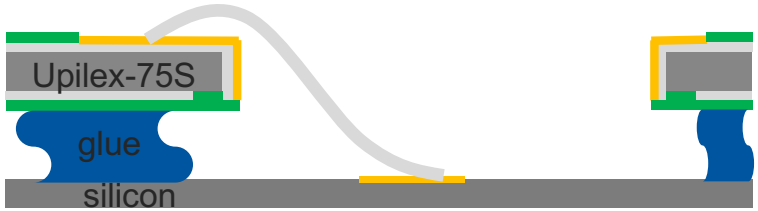
Glue deposition on FPC (Ablestik 45 W)



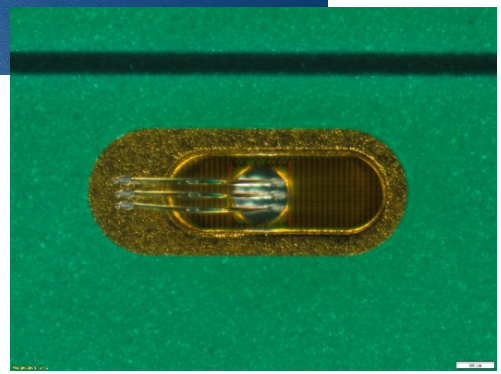
FPC+chip connection and curing (RT for 12h)

IB HIC ready for wire bonding



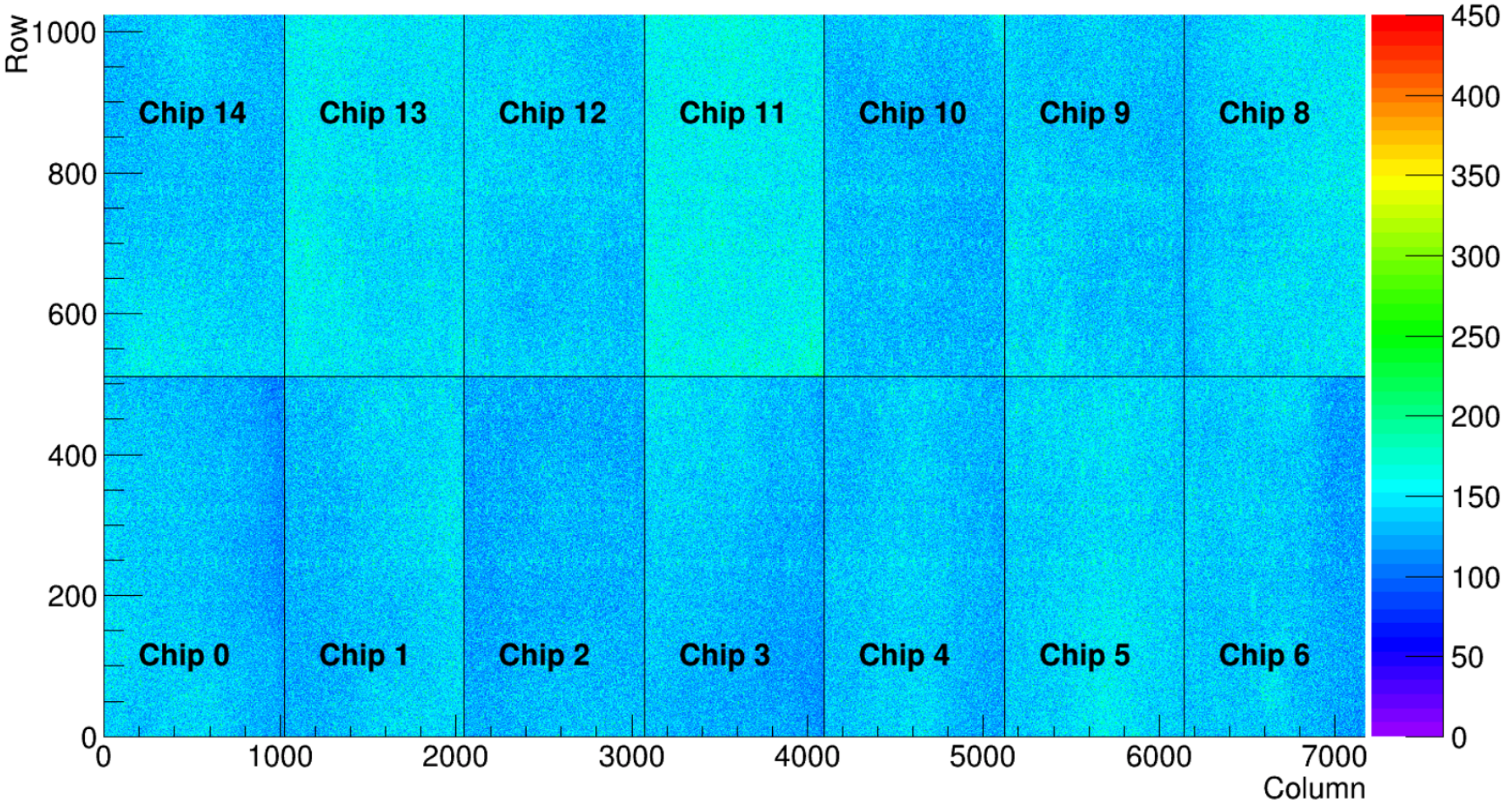


Wire bonding



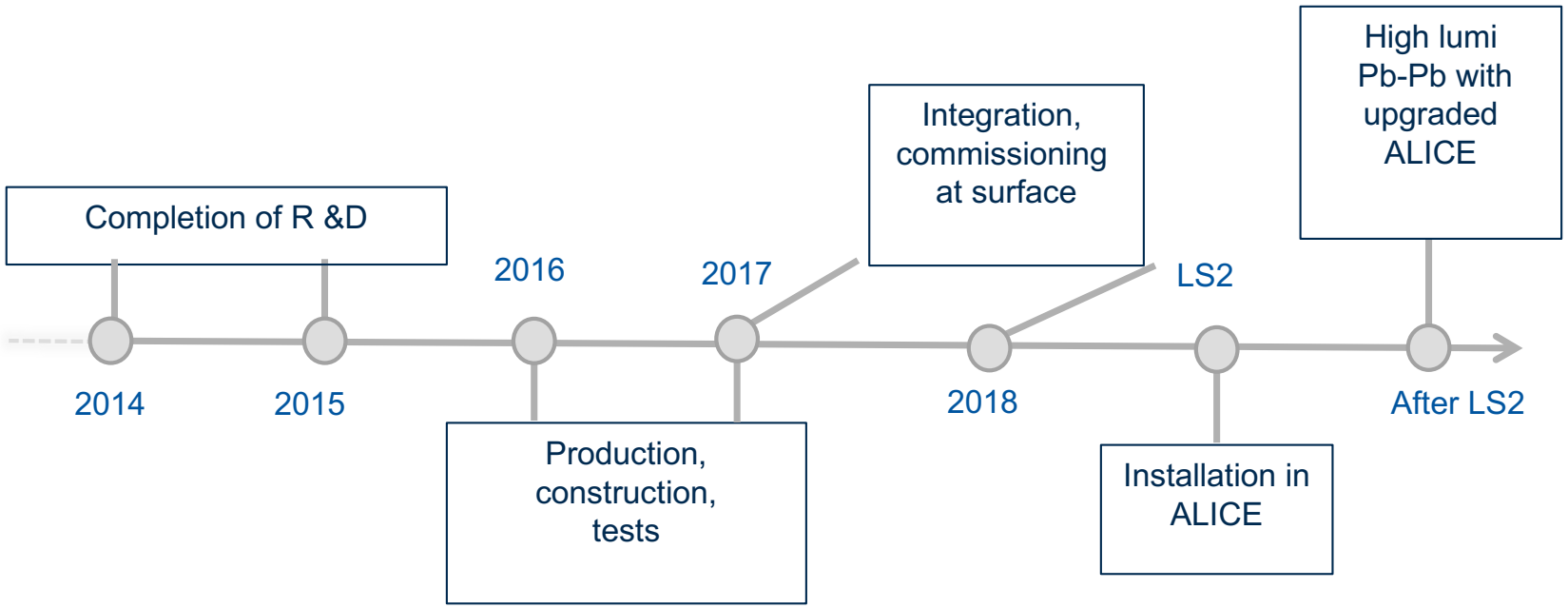
HIC

Electrical characterisation, e.g. threshold scan carried out after full assembly.
Example: OB HIC



M. Keil, HIC and Stave PRR

Timeline ALICE ITS



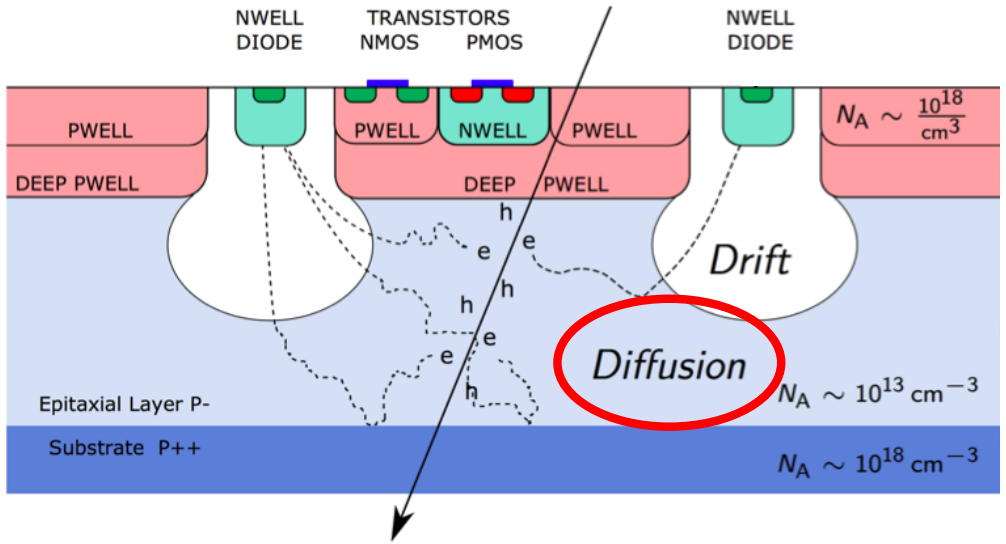
Production of components (chips, etc.) has already started and the HIC production is about to commence (PRR yesterday).

MAPS in Future Experiments

Present MAPS offer a number of very interesting advantages, but the diffusion is a limiting factor.

In a (very) high radiation environment (10^{15}-10^{16} n_{eq}/cm^2):

- The ionization charge is trapped/recombined in the non-depleted part → no more signal.
- Diffusion makes signal collection slower than typical requirements for pp-colliders.



Readout architectures are low power, but not designed for high rates like p-p at LHC.

Challenges for the Future

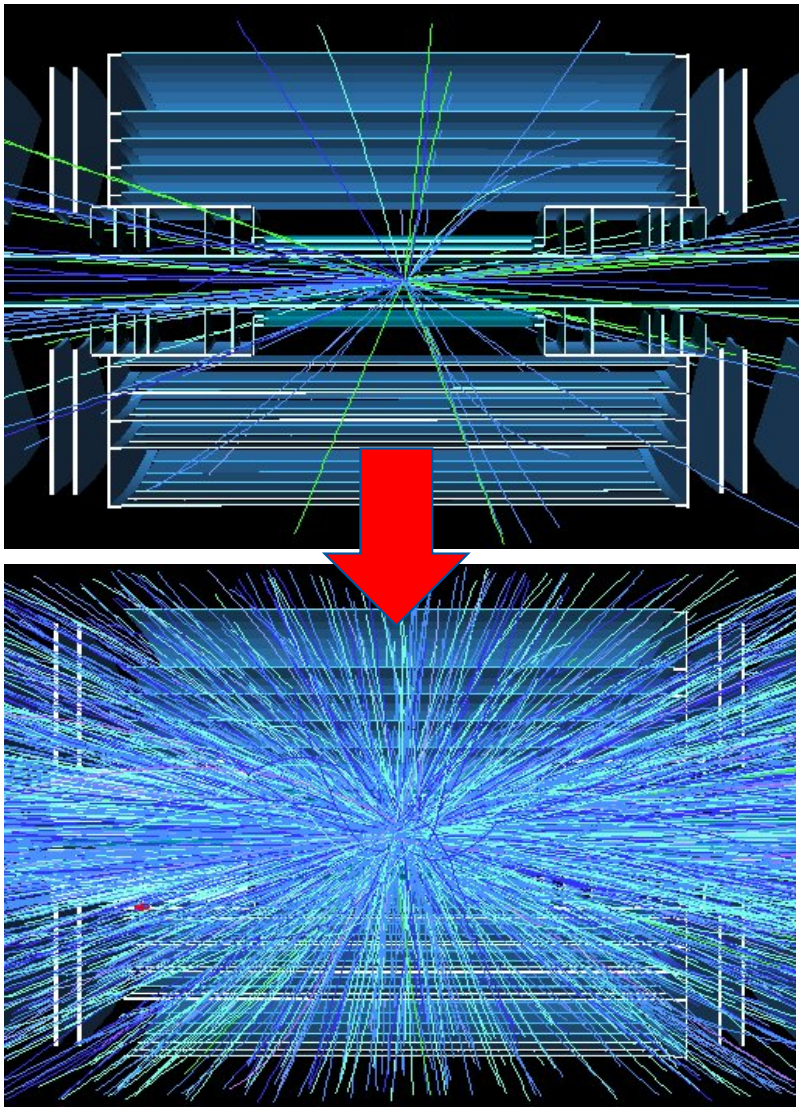
Increased luminosity requires

- Higher hit-rate capability
- Higher segmentation
- Higher radiation hardness
- Lighter detectors

Radiation hardness improvement compared to now

- Phase-2 approx. factor 10-30

Can MAPS be ready for this environment?



MAPS for the Future

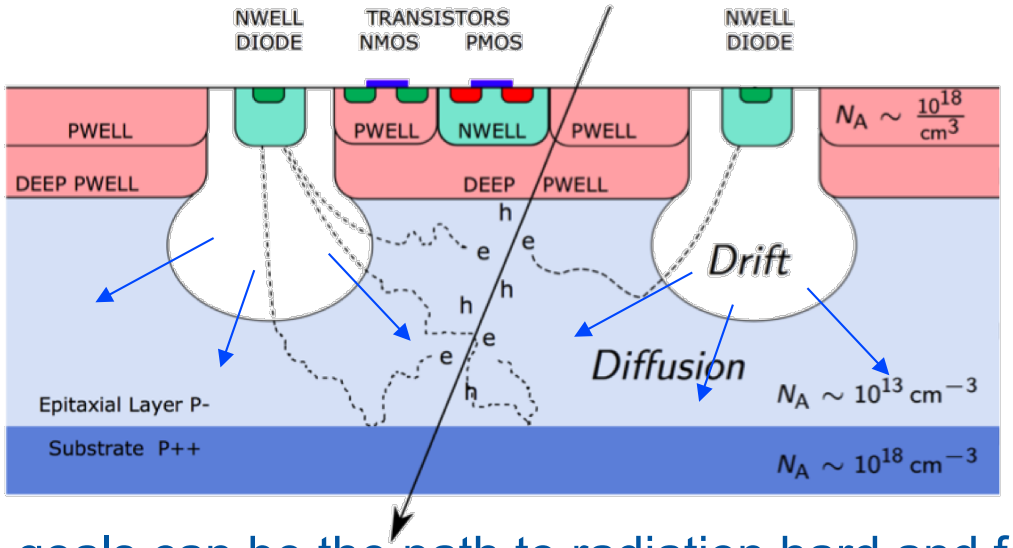
The ALPIDE has demonstrated that partial depletion extends the operability of MAPS to the radiation levels of ALICE.

Depletion will allow to collect charges by drift and not diffusion :

→ reduce charge trapping/recombination (10^{15}-10^{16} n_{eq}/cm^2)

→ faster signal collection (25 ns BC)

In addition, the **design** needs to be adapted to meet the specifications.



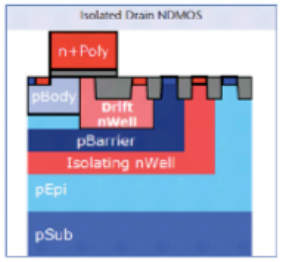
Achieving these goals can be the path to radiation hard and fast CMOS sensors.

MAPS for the Future

Different types of MAPS are under study, with the aim to achieve radiation hardness through depletion, high rate capability, low power, …..

Enabling technologies are now available, which were not there some years ago ,e.g.:

"High" Voltage add-ons	Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm).
"High" Resistive Wafers	8" hi/mid **resistivity** silicon wafers accepted/qualified by the foundry. Create depletion layer due the high resistivity.
Technology features (130-180 nm)	Radiation hard processes with **multiple nested wells.** Foundry must accept some process/DRC changes in order to optimize the design for HEP.
Backside Processing	Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing.



from: www.xfab.com

Depletion and Fill Factor

To better **deplete the active volume**:

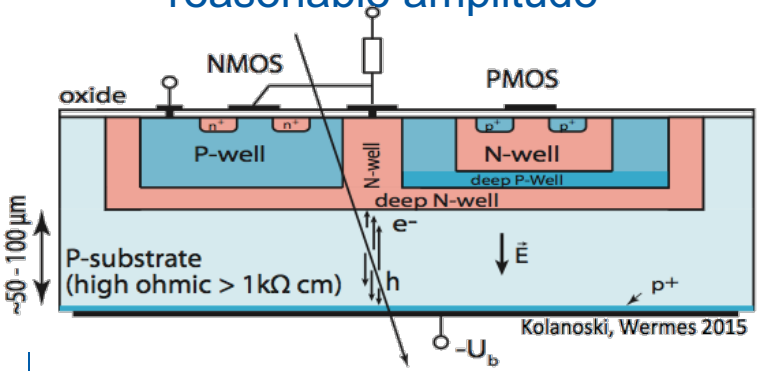
- Use high resistivity (epi) wafers (~kOhmcm)
- Apply bias voltage

$$d \propto \sqrt{\rho V}$$

The **fill factor** will affect how the depletion region grows:

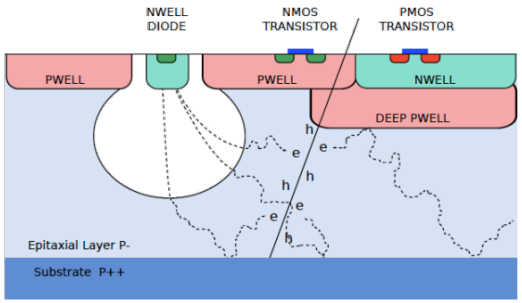
Large fill factor

- Uniform charge collection
- Large capacitance (~50-200 fF) on CSA
- More power necessary to achieve fast signals with reasonable amplitude



Small fill factor

- Higher gain and faster response due to smaller capacitance (2-5fF) and higher Q/C
- Potentially lower power consumption
- Signal collection under DPW after irradiation more difficult on edges



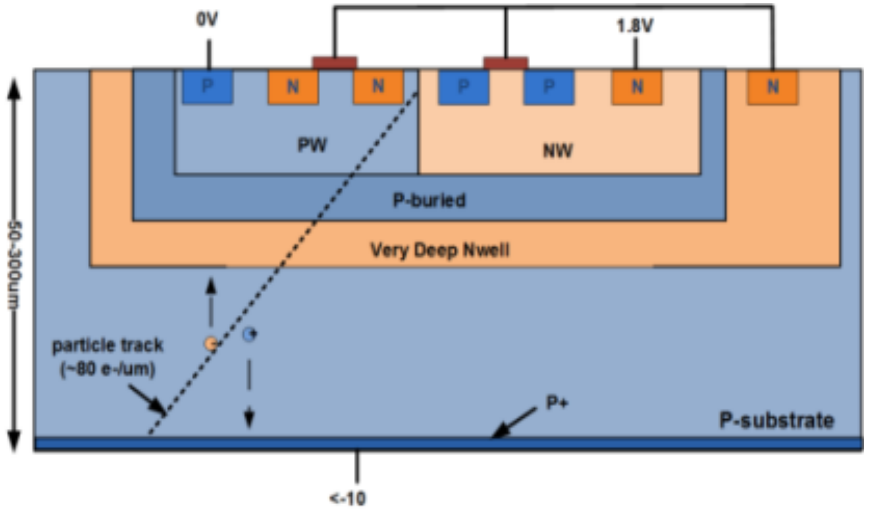
Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

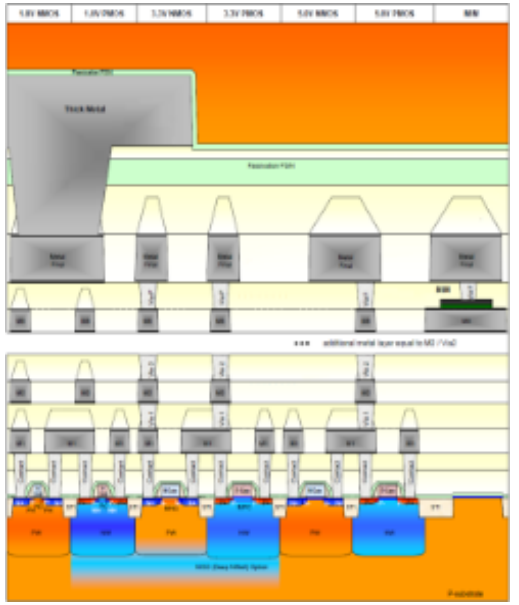
Examples: Large Fill Factor

An example of large electrode pixel sensors are the development lines in the LFoundry and in AMS processes.

LFoundry:

- L-Foundry 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Resistivity of wafer: **>2000 Ω·cm**
- Small implant customization
- Backside processing





P. Rymaszewski et al., JINST 11 (2016) 02 C02045
T. Hirono et al., doi:10.1016/j.nima.2016.01.088

universitätbonn

LFoundry Development Line

CCPD_LF

- Subm. in Sep. 2014
- 33 x 125 µm^2 pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test
- ***(Almost) Fully characterized***

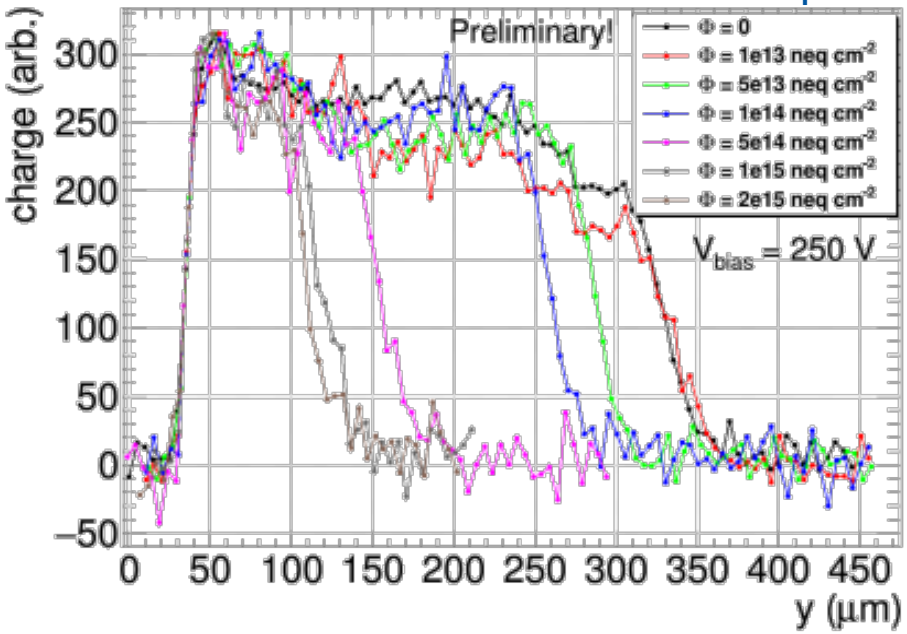
LF-CPIX (DEMO)

- Subm. in Mar. 2016
- ***CPIX demonstrator in LF***
- 50 x 250 µm^2 pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test
- ***First meas. available***

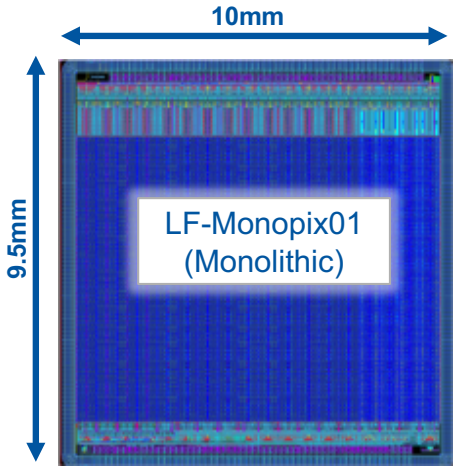
LF-Monopix01 (monolithic)

- Subm. in Aug. 2016
- "Demonstrator size"
- 50 x 250 µm^2 pixels
- ***Fast standalone R/O***
- Standalone R/O like LF-CPIX

Edge TCT on neutron irradiated CPIX sensors up to 2x10^{15} neq/cm^2



I. Mandic, B. Hiti (Ljubljana)



AMS Development Line

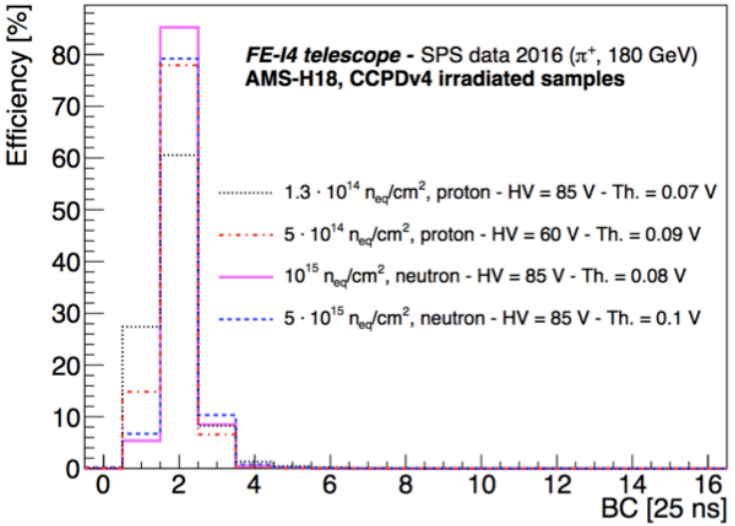
Capacitively Coupled Pixel Detectors (H18 AMS process)

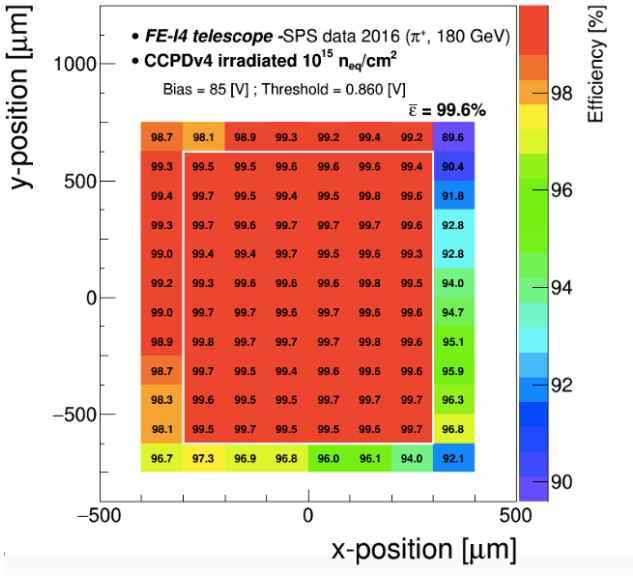
- Capacitive-Coupling of CMOS sensor to ATLAS FEI4 (sensor pixel size 33x 125um2)
- Blocks for monolithic design implemented an studied (DAC,Amplifier, Discriminators, Configuration)
- Efficiency of > 99.5%
- Signal collected in 3BC

T. Weston/ Uni Bern @ TREDI 2017
Mathieu Benoit / Uni Geneve

H18 CCPDv5

- First prototype in aH18 process (Hi-Resistivity wafer processing)
- Many beam tests carried out to test operation, tuning, achievable threshold and efficiency
  - 600-650e Threshold





Example: Small Fill Factor

Small input capacitance of few fF compared to hybrid pixels (O (100fF, IBL))* or large fill factor MAPS → beneficial for timing, noise and power!

1. Input capacitance drives peaking time and ENC → low input capacitance will reduce peaking time and ENC

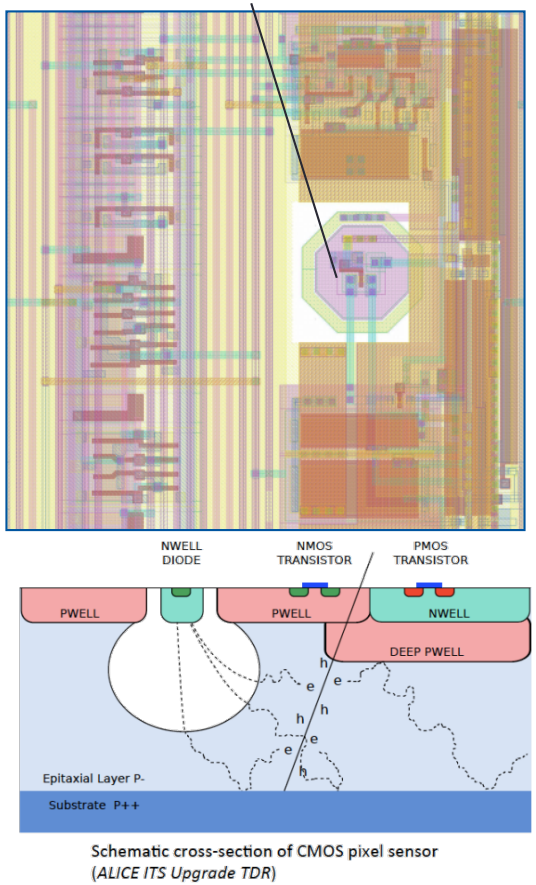
2. Analog power: depends on collected charge over capacitance Q/C in the pixel → optimize sensing node**

$$P \sim \left\{ \frac{S}{N} \frac{Q}{C} \right\}^{m} \quad with\ 2 \leq m \leq 4$$

But collection underneath deep p-Well is limited due to depletion limit…

Collection diode ~ 2-3 µm ø, C~ O(few fF)
27 µm x 29 µm pixel

T. Kugathasan, W. Snoeys

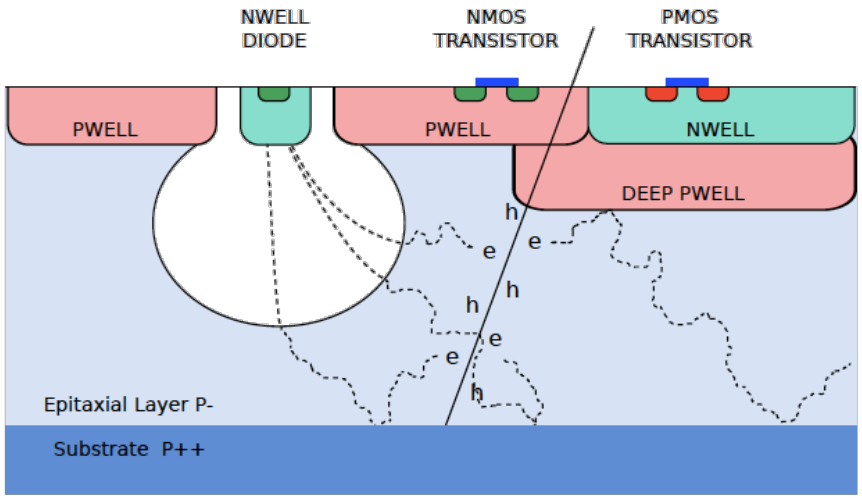


Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

*Havranek et al, NIMA 714 (2013) 83-89

** W. Snoeys, NIM. A765 (2014) 167-171

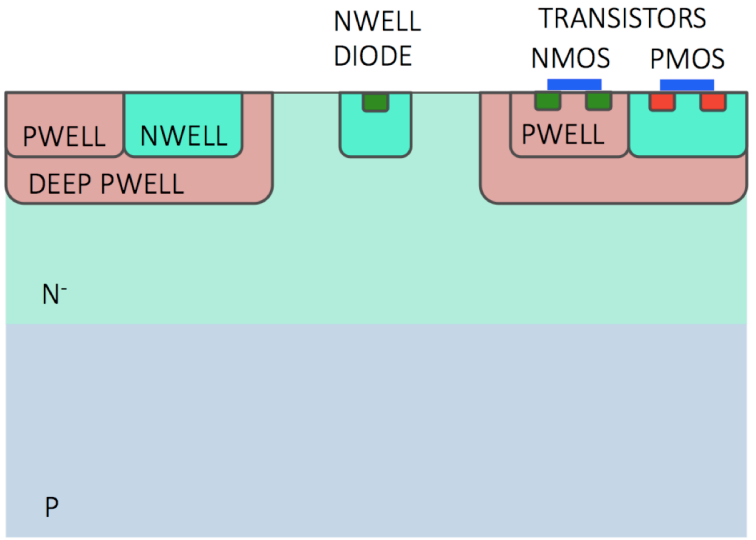
Modified TowerJazz Process



Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

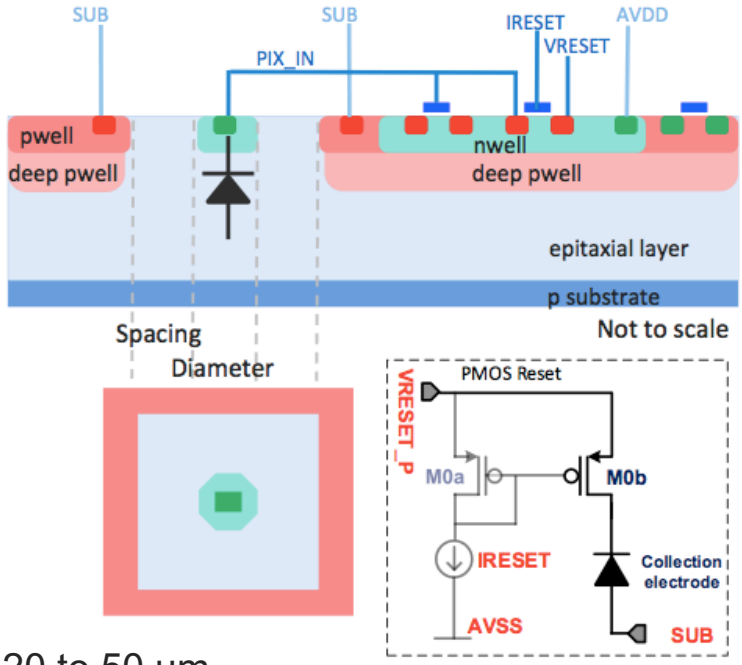
- **Small collection electrodes**
  - Higher gain and faster response due to smaller capacitance (~5fF) and higher Q/C
  - Potentially lower power consumption
  - Signal collection under DPW after irradiation more difficult on edges

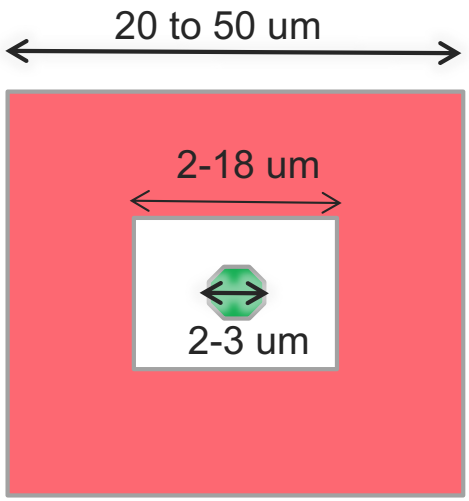
- **Modified Process**
  - Add planar n-type layer
  - Significantly improves depletion under p-well with deep junction
  - Does not require significant circuit or layout changes



L. Musa, ECFA High Luminosity LHC Experiments Workshop - 2016

TowerJazz 180nm Investigator





- **Pixel dimensions for the following measurements:**
- 20x20 to 50x50um^2 pixel size
- **3 um diameter electrodes** 25um EPI layer

Designed as part of the ALPIDE development for the ALICE ITS upgrade

Emphasis on small fill factor and small capacitance enables low analog power designs (and material reduction in consequence)

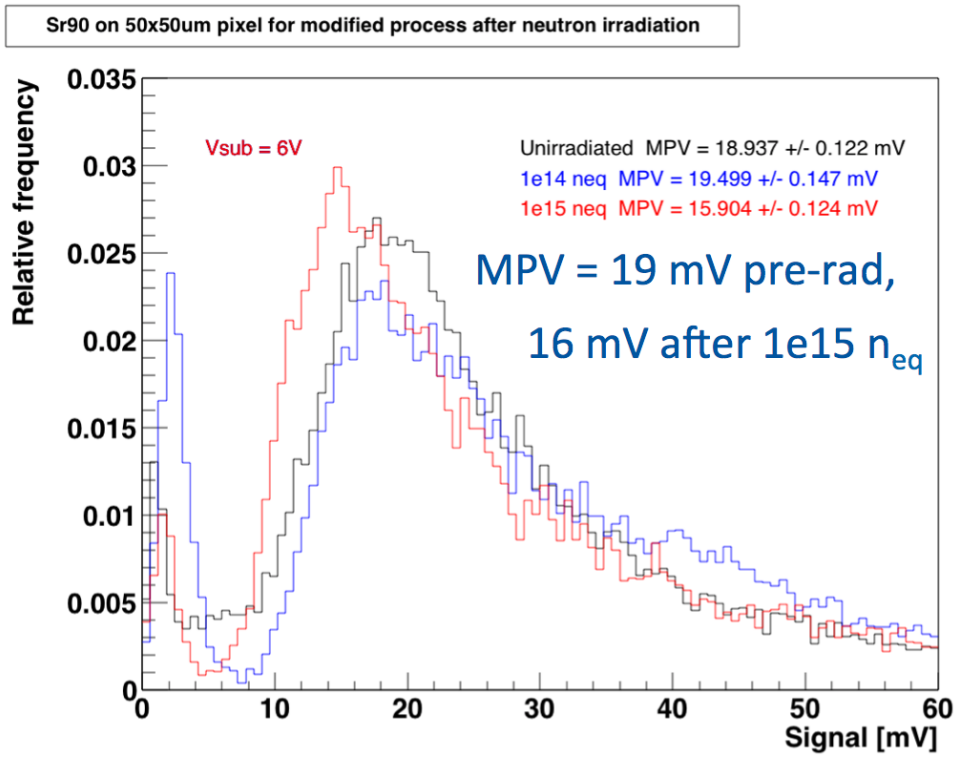
C. Gao et al., NIM A (2016) 831
http://www.sciencedirect.com/science/article/pii/S0168900216300985

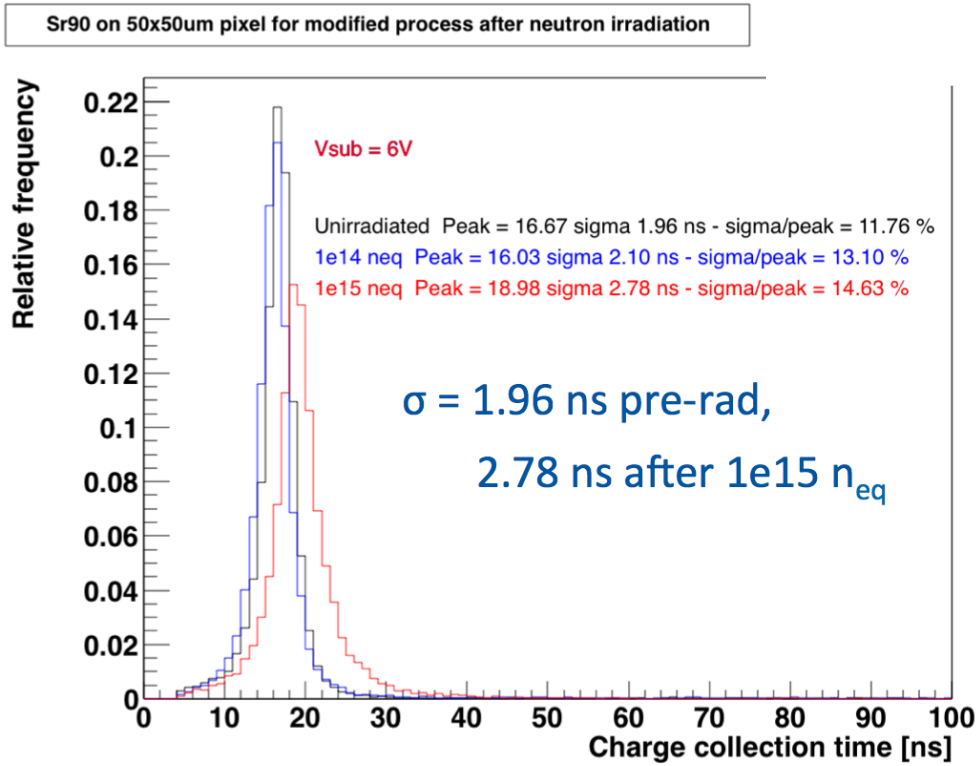
J. Van Hoorne, proceedings of NSS2016
http://2016.nss-mic.org/nss.php

Produced in TowerJazz 180nm on 25-30um thick epi layer in the modified process

Design: C. Gao, P. Yang, C. Marin Tobon, J. Rousset, T. Kugathasan and W. Snoeys

After 10^{15} n_{eq}/cm^2 and 1Mrad TID





Very little signal loss after 10^{15}, also very encouraging results on detection efficiency.
Signal well separated from noise.
Measurements on samples irradiated to 10^{16} n_{eq}/cm^2 ongoing.

H. Pernegger, Terascale Detector Workshop, DESY, April 2017

Next Step

- Investigator measurements after 10^{15} n_{eq}/cm^2 very encouraging
- Small fill factor design in modified TowerJazz 180 nm process is very promising for higher radiation levels

Submission of full-size monolithic sensor chip matching the ATLAS specs in the modified process of TowerJazz:

- Analog front-end with CSA+discriminator optimized for 25 ns in-time efficiency and low threshold operation
- 2 x 2 cm^2 chip size with <50 x 50 μm^2 pixels
- Monolithic design includes readout architecture which copes with ATLAS outer layer hit rate requirement

H. Pernegger, Terascale Detector Workshop, DESY, April 2017

TowerJazz Submission May 2017

TJ MALTA

Full matrix = 512x512 pixels

Design/CERN

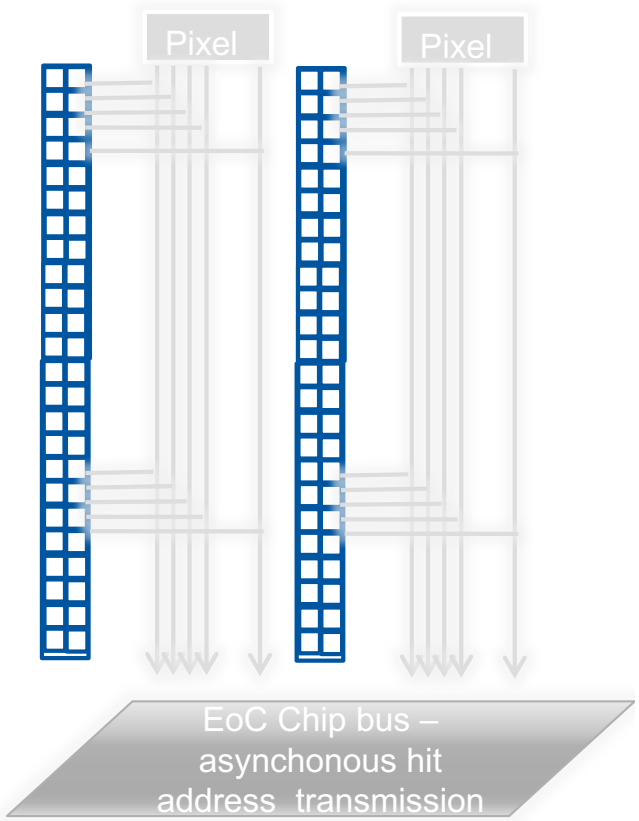
- Active area 18 x 18 mm^2
- Hit memory in active matrix
- All hits are **Asynchronously transmitted over high-speed bus** to EoC logic
- **No clock distribution over active matrix** to minimize power and digital-analog cross-talk

TJ MonoPix

512x256 pixels

Design/Bonn/CERN

- Active area 18 x 10 mm^2
- Hit memory in active matrix (2 flip-flop per pixel)
- **Synchronous column drain architecture**
- Hit address asserted to bus with 40MHz token
- 6 bit ToT coding at end of column



Design Team: W. Snoeys, T. Kugathansan, C. Marin Tobon, I. Berdalovic, R. Cardella, N. Egidos (CERN) J. Rousset, B. Blochet (MIND), T. Hemperek, K. Moustakas, T. Wang (Bonn)

Summary

- The development of monolithic active pixel sensors have made significant progress in the last years.
- The STAR HFT pixel upgrade and the ALICE ITS upgrade are entirely based on MAPS.
- A lot of work is being done to make MAPS an attractive option for high rate and high radiation environments.
- We can expect some exciting results from new chips in the next months and will look out for new module assembly and interconnection ideas!

Acknowledgements

Many thanks to all who have kindly provided me with material, discussions and help for this presentation:

Luciano Musa, Antonello di Mauro, Jacobus v. Hoorne, Antoine Junique, Markus Keil, Walter Snoeys, Leo Greiner, Heinz Pernegger, Werner Riegler, Norbert Wermes, my colleagues from the ALICE ITS and from STREAM !